

17.4GHz Ultra-wideband Digital Correlator in NTU-Array

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Outline

- NTU-Array Correlator Architecture
 - NTU-Array
 - Front-end ADC
 - Tbps real-time DSP system
- Testing method and Results
 - Digital system test
 - Correlator full-system verification

NTU-Array

Science target:

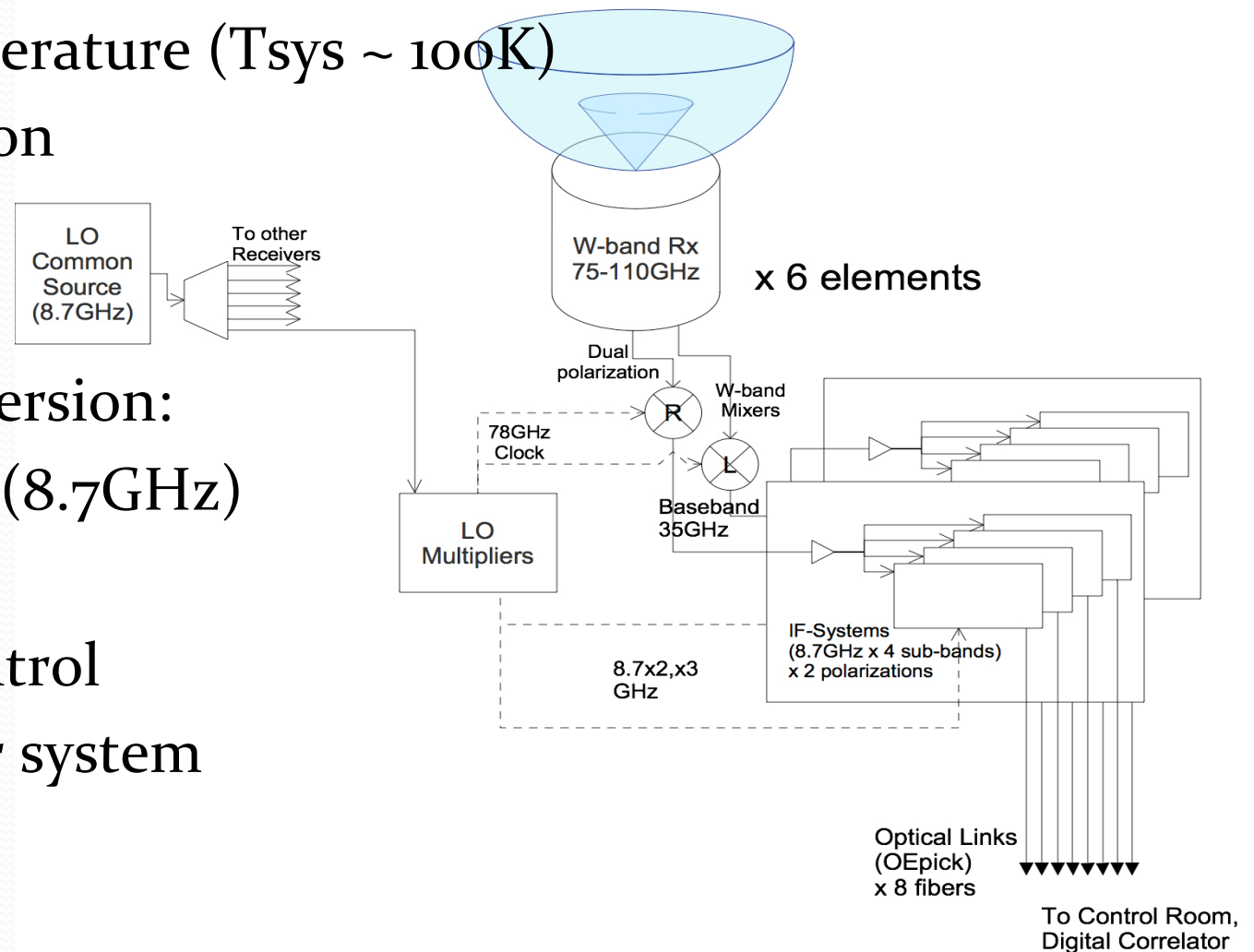
CMB primary and secondary
anisotropies cross-over



NTU-Array: Receiver and RF system

- 6 receivers
 - 35GHz BW(78-113GHz)
 - low noise temperature ($T_{\text{sys}} \sim 100\text{K}$)
 - dual-polarization

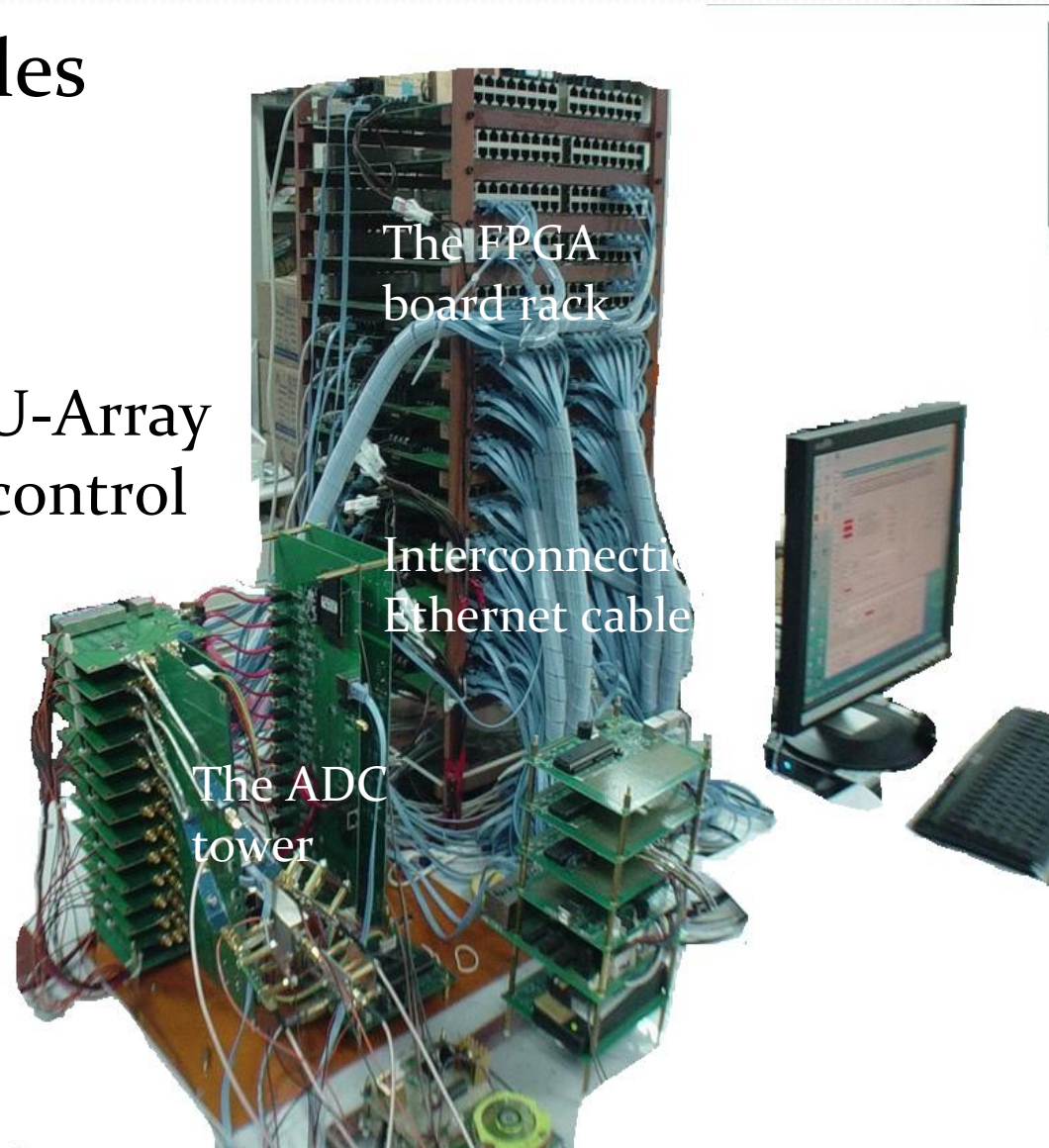
- LO-IF down-conversion:
RF \rightarrow 4 IF-bands (8.7GHz)
- Optical link:
telescope \rightarrow control
room/correlator system



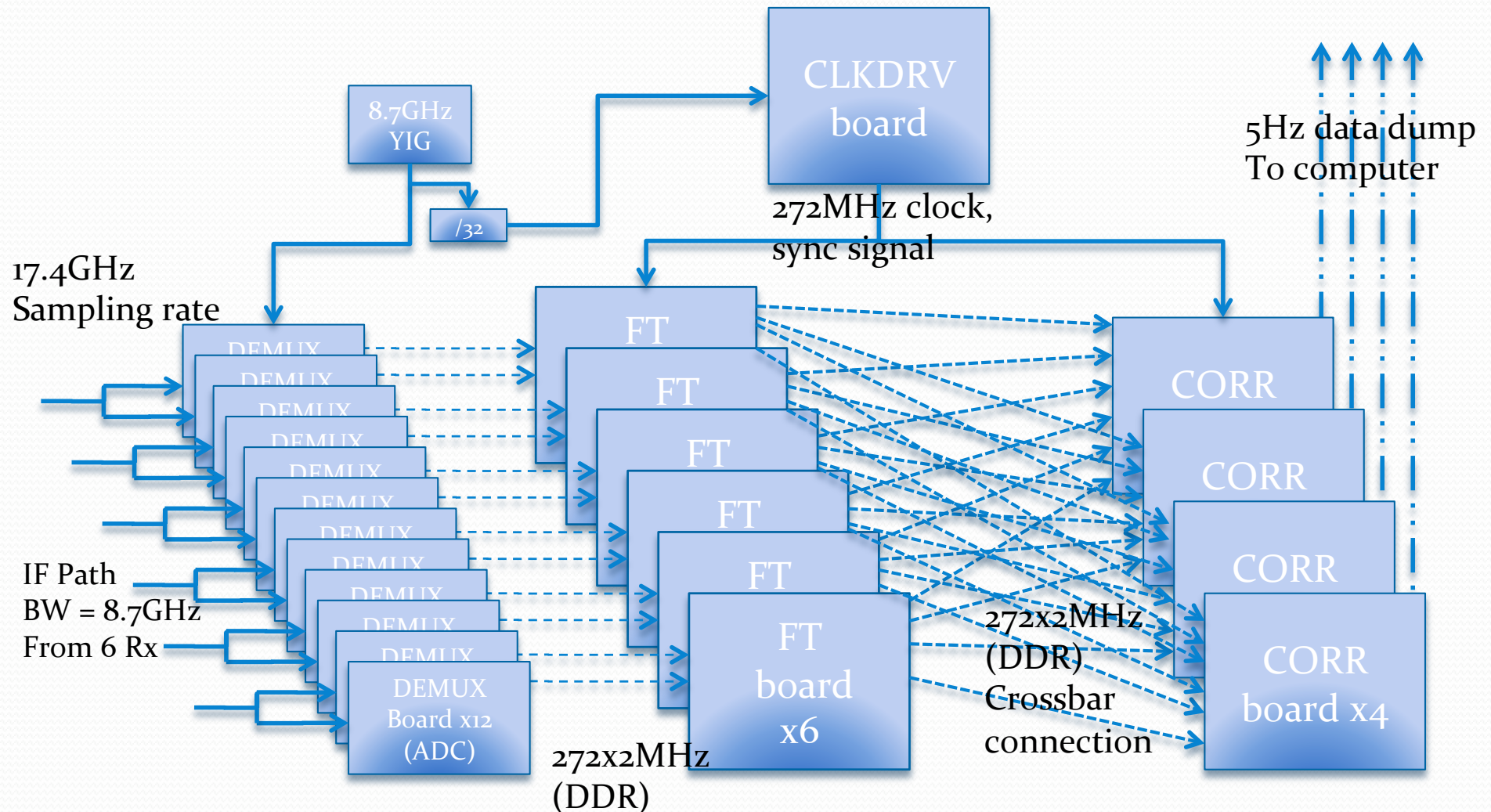
NTU-Array Correlator System

- 8 identical modules for 2 polarization

One module of NTU-Array correlator with the control terminal



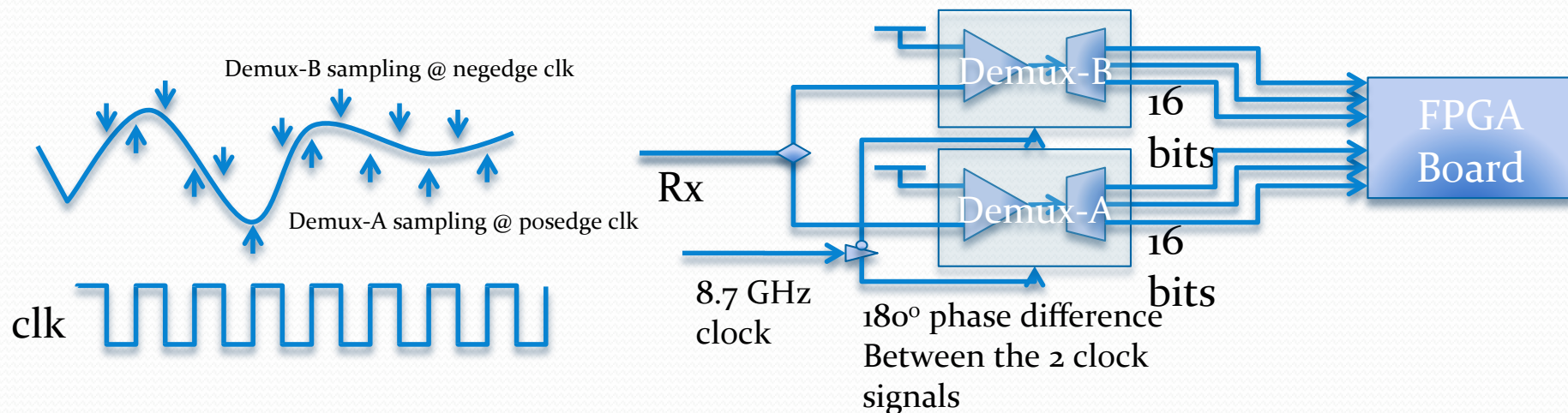
Block Diagram for 1 correlator module



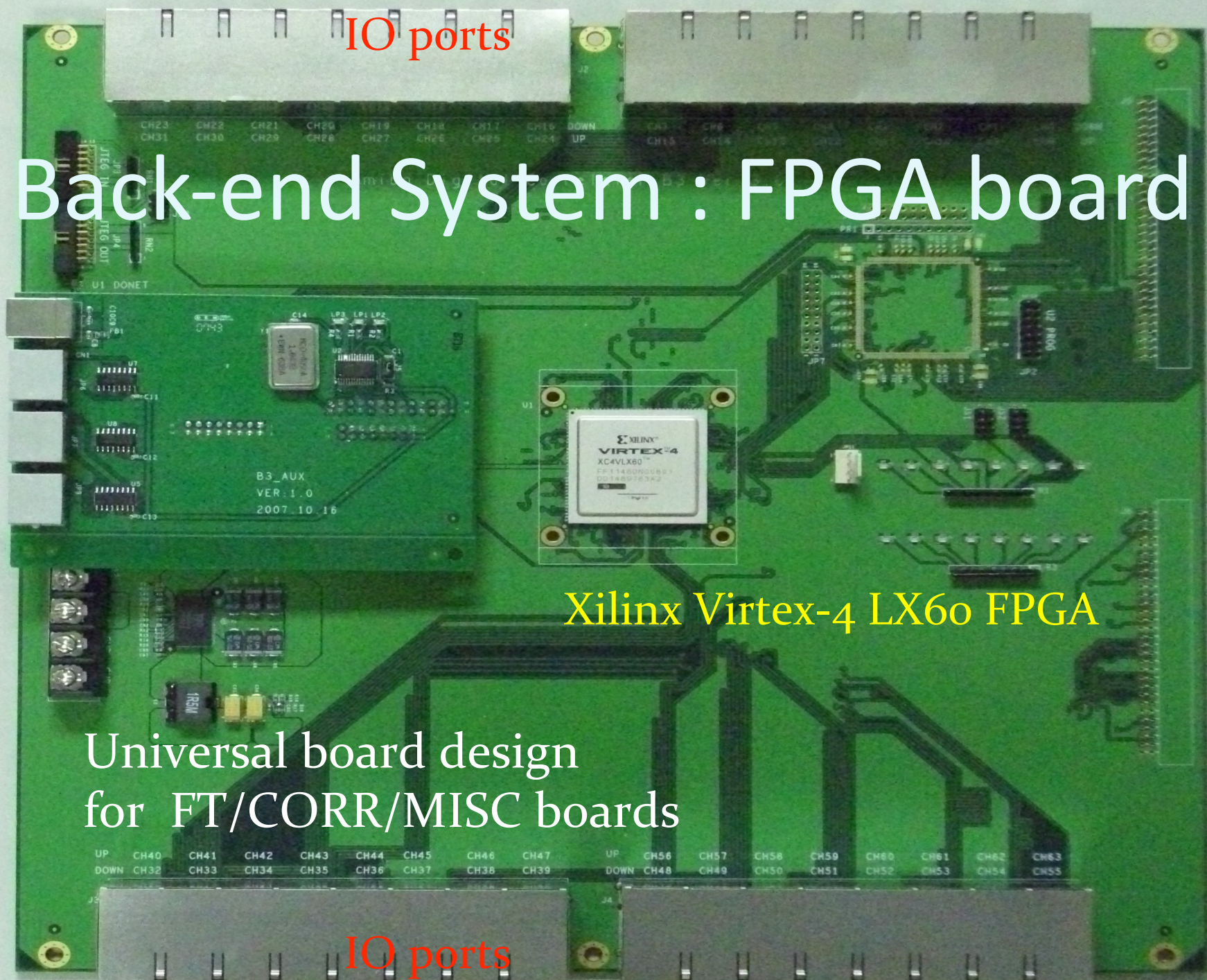
Front-end System:

1-bit ADC (Maxim 3950)

- 2-way interleave sampling
- 1-bit digitization
 - by Demux CML input comparator & latch
- Parallelize => 32-bit data-buses @ 544MHz



- 3-bit 20GHz ADC under develop



IO ports

Back-end System : FPGA board



Xilinx Virtex-4 LX60 FPGA

Universal board design
for FT/CORR/MISC boards

UP CH40 CH41 CH42 CH43 CH44 CH45 CH46 CH47 UP CH56 CH57 CH58 CH59 CH60 CH61 CH62 CH63
DOWN CH32 CH33 CH34 CH35 CH36 CH37 CH38 CH39 DOWN CH48 CH49 CH50 CH51 CH52 CH53 CH54 CH55

IO ports

Back-end : real-time DSP

- 88 FPGA boards
- optimized for short word-length arithmetic & logic operation
- 40T fixed-point arithmetic op/sec
- Aggregate Comm. BW = 4 Tbit/s
- Power consumption: < 1200W

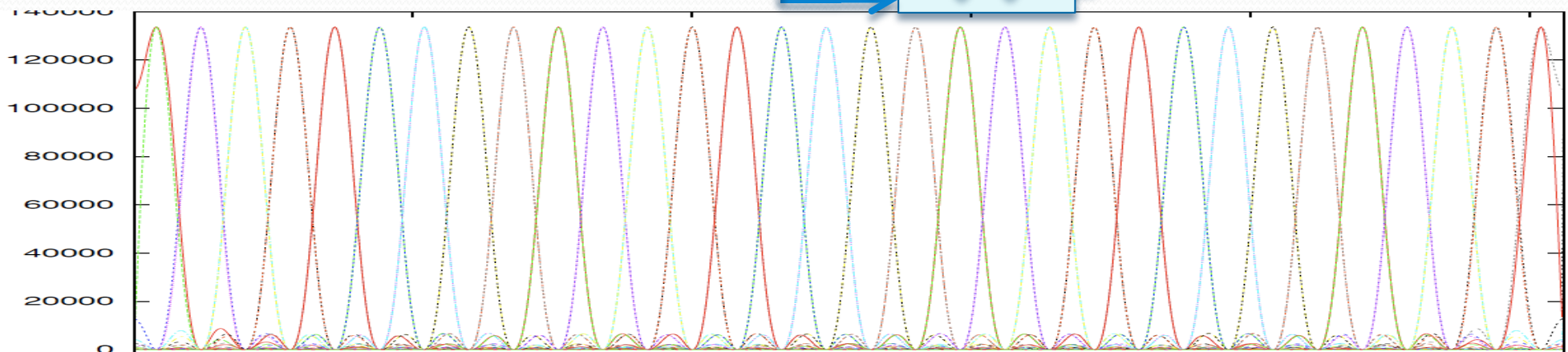
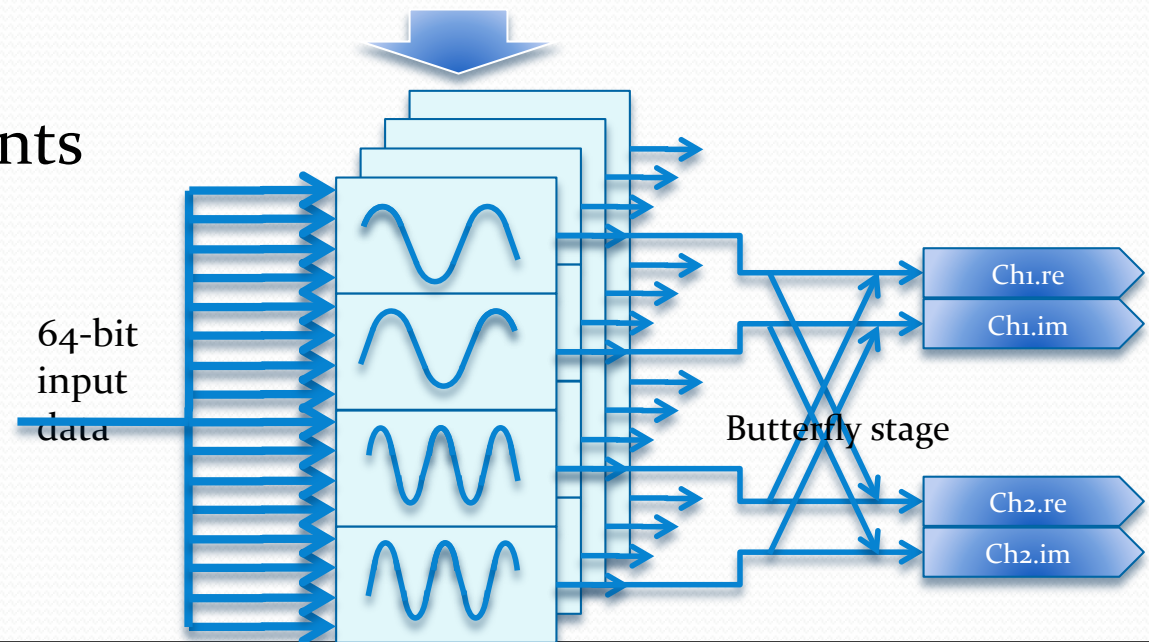
Interconnection

- SI issue & phase variance
- Auto-alignment scheme:
 - programmable tap delay lines & shifter registers
- PRBS check result : BER < 10^{-7} at 544MHz

Frequency Filter Boards

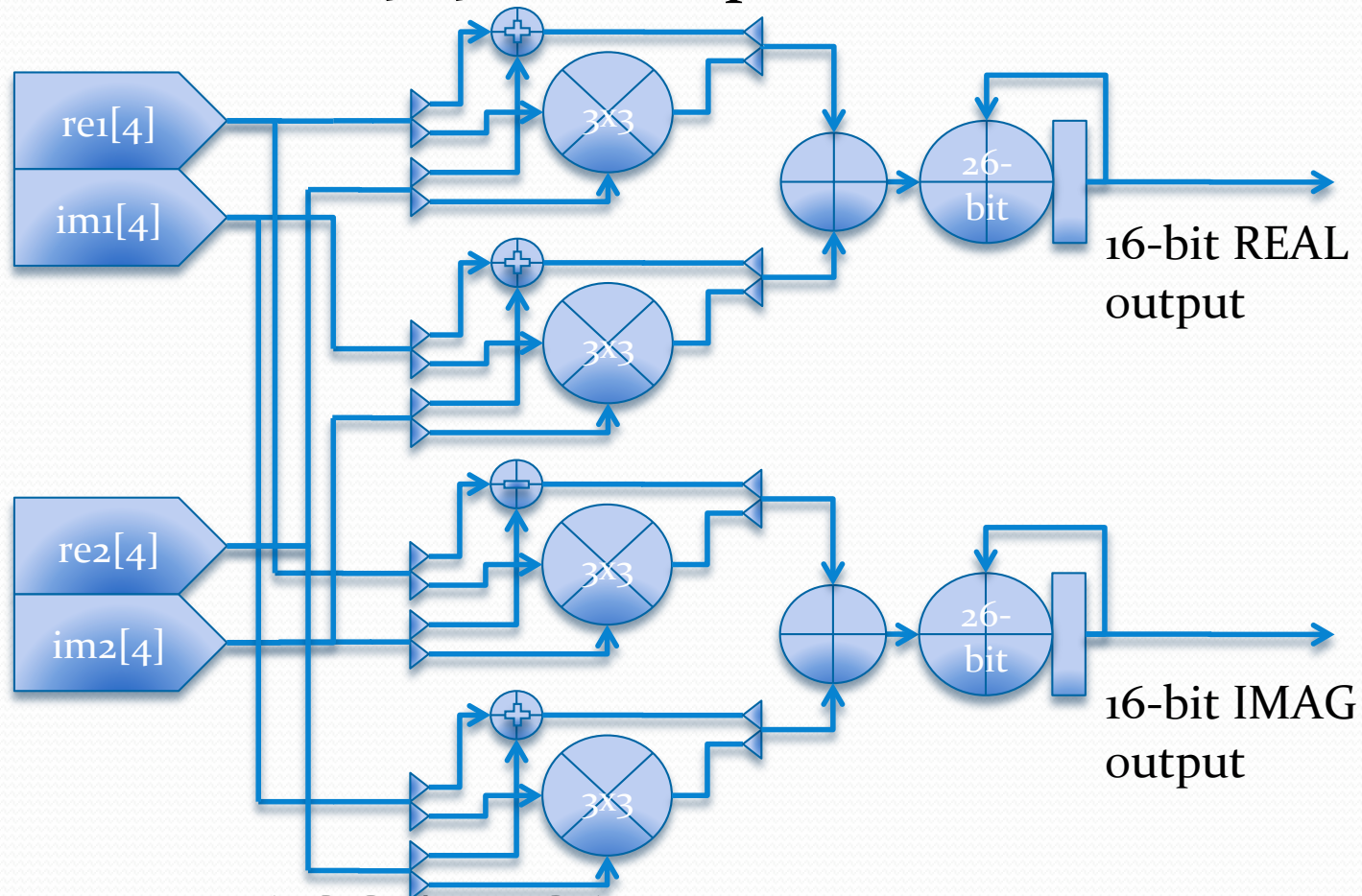
- No FIR filter ahead
- precision
 - 4-bit filter coefficients
 - 4-bit decimation for freq components
- band-pass filters:

32(channels)x2(complex) filters
(4-bit precision, length=32)



Cross Correlation Boards

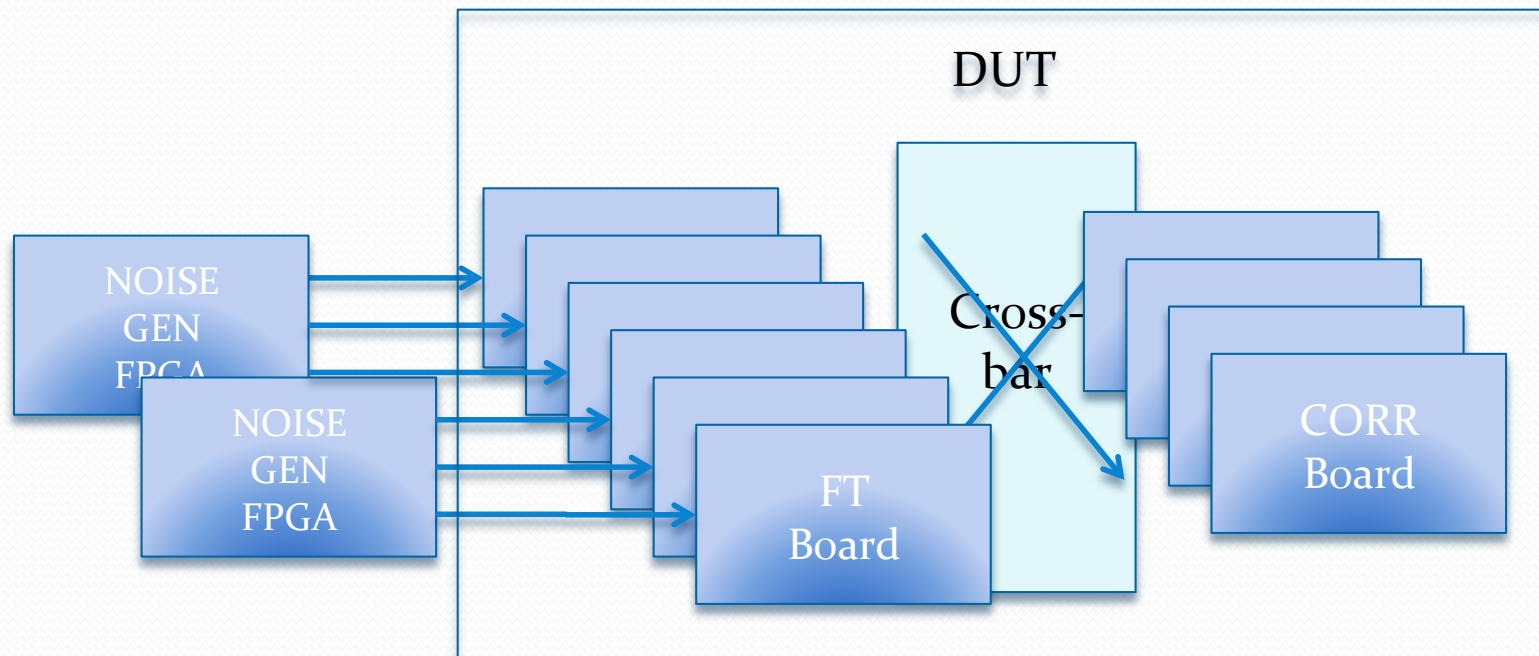
- Basic module: 4x4-bit complex MUL/26-bit ACC



- 120 cplx MACC / FPGA
- data reduction: dump rate = 5Hz

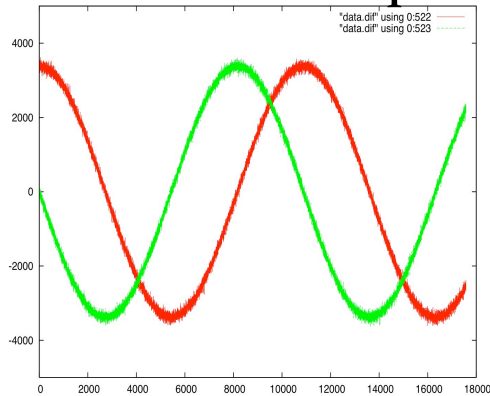
Digital system Testing

- 121- to 126-bit PRBS generators
 - Digitized AWGN (period $> 10^{25}$ sec)
- small correlated signals inserted : SNR = 1/256
 - dynamic delay shifting => artificial fringes

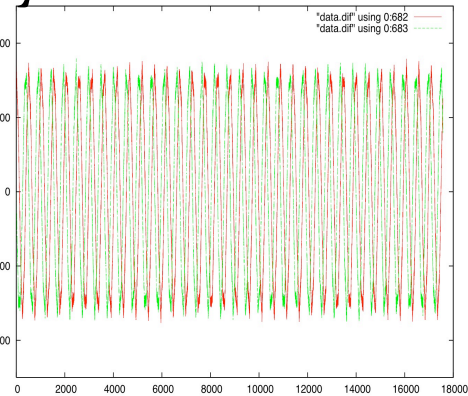


Testing results: comparison between channels

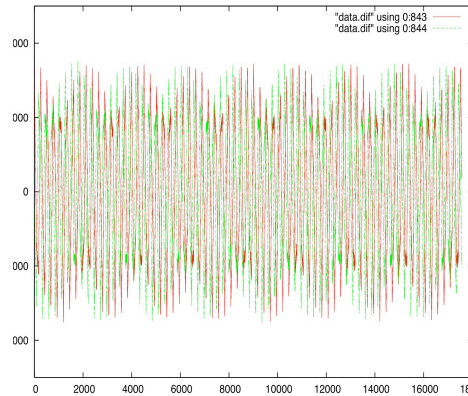
Different frequency channels:



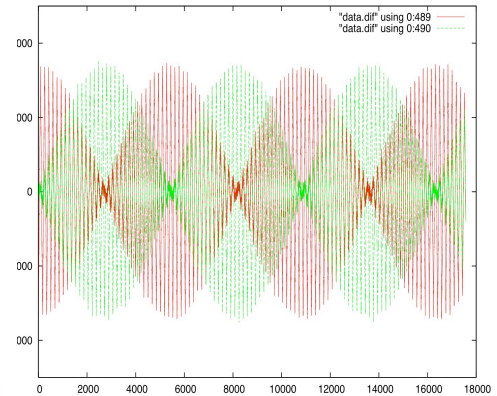
Ch. 0, $f_0=136\text{MHz}$



Ch. 10, $f_0=2.85\text{GHz}$

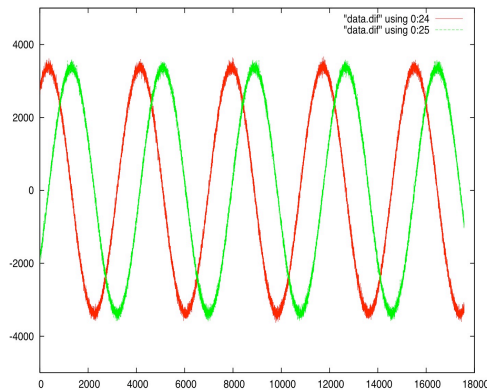


Ch. 20, $f_0=5.57\text{GHz}$

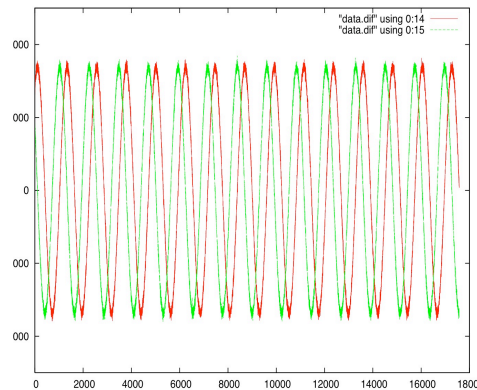


Ch. 31, $f_0=8.56\text{GHz}$

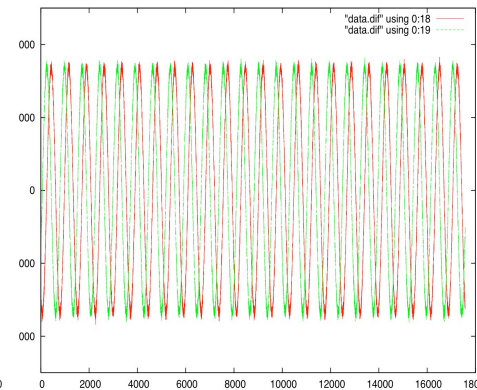
Different pairs with various fringe periods:



Rx4 x Rx3 Ch.1



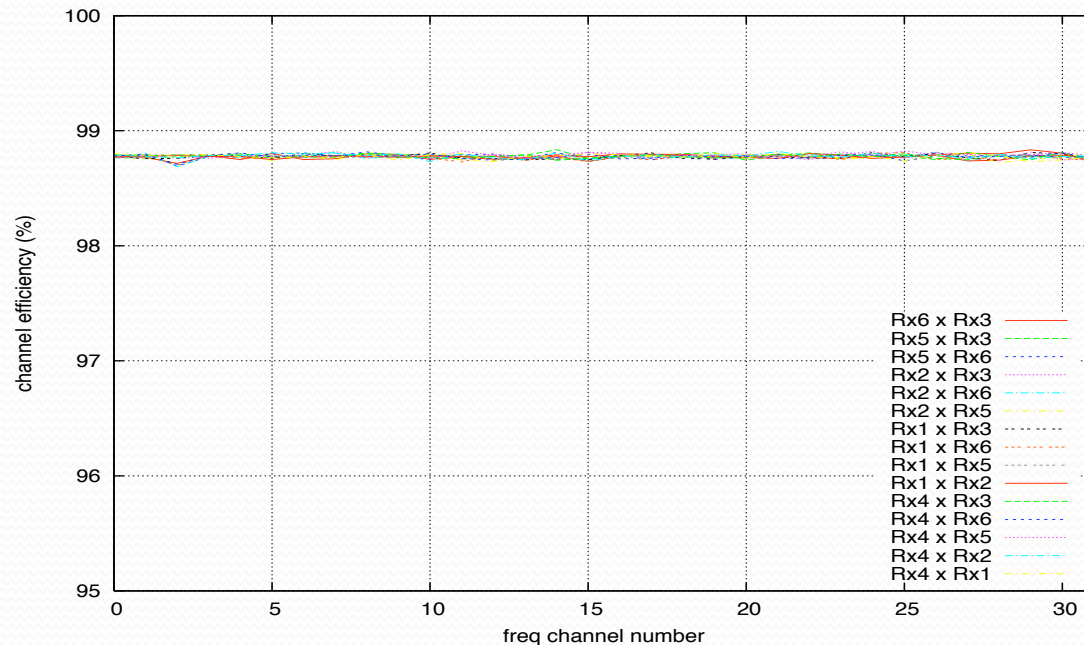
Rx2 x Rx5 Ch.1



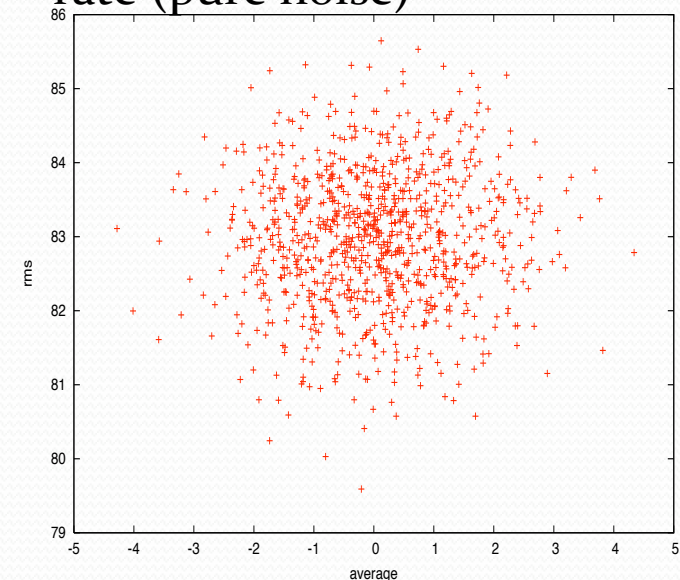
Rx1 x Rx6 Ch.1

Testing results : SNR

- The SNR of all the 480 channels in one module is calculated from amplitude fitting of the artificial fringes
- All the channels give $\sim 98.8\%$ consistent efficiency (due to 4-bit decimation)

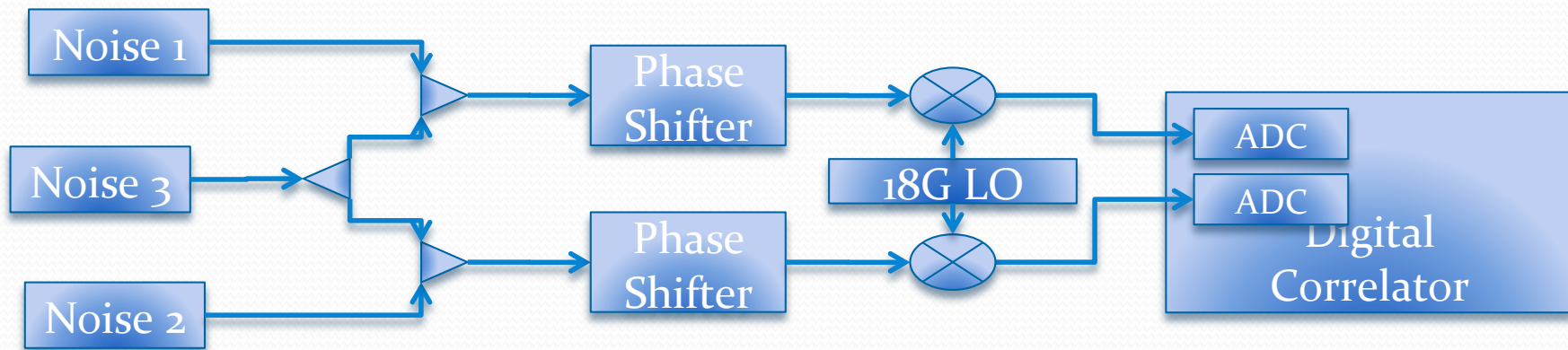


rms and average distribution of correlation data at 5Hz dump rate (pure noise)



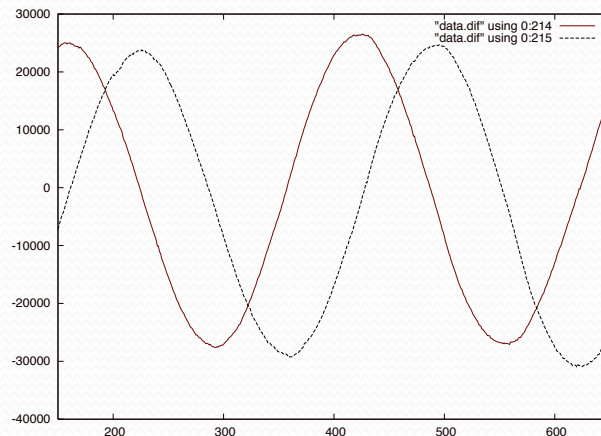
Performance verification: full-system

- Broad-band noise & signal input (9-18GHz)

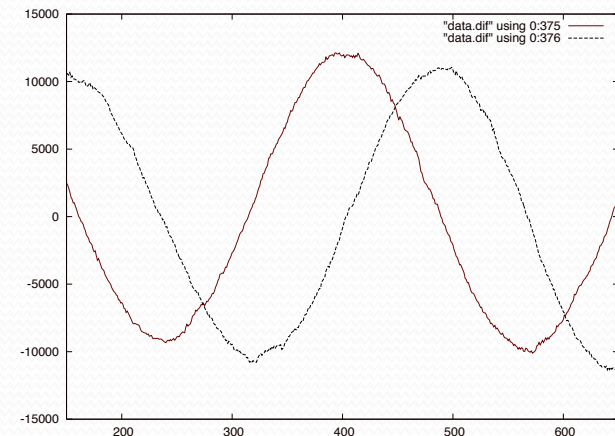


Results:

3.67GHz



6.39GHz



Expansibility

- Switchable operation modes
 - $X_1 * X_2 + Y_1 * Y_2$: I parameter
 - $R_1 * L_2$, $L_1 * R_2$: Q,U parameter
 - $R_1 * L_1$: gain calibration
- Scalable to 16 receiver arrays
- Finer spectrum resolution
 - Additional FFT stage : 4k channels
 - FIR filters



Thank You!