Chapter 1

1. With a 1 on the upper input and a 0 on the lower input, all circuits will produce an output 0. If instead a 0 is on the upper input and 1 is on the lower input, circuits b and c will produce an output 1, and circuit a will still produce a 0.

4. This is a flip-flop that is triggered by 0s rather than 1s. That is, temporarily changing the upper input to 0 will establish an output of 1, whereas temporarily changing the lower input to 0 will establish an output of 0. To obtain an equivalent circuit using NAND gates, simply replace each AND-NOT gate pair with a NAND gate.

5. Address Contents

00	02
01	53
02	01
03	53

7. a. 100010101001 b. 110111001011 c. 111011110011 d. 101000000001 e. 110010011001

9. a. B4B4B b. 1E1 c. FEDB

11. 262,144. (Each pixel would require four memory cells.)

15. The document would require about 0.8MB if two byte Unicode characters are used.

18. Only 400KB!

24. a. 001100000010111100101111 b. 11111111

26.

	Binary	base 10 representation
a.	00001010	10
b.	00010100	20
c.	00011110	30
d.	00101000	40
e.	00110010	50
f.	00111100	60
g.	01000110	70
h.	01100101	101
i.	11001010	202
j.	0000000100101111	303
k.	0000000110010100	404
l.	0000000111111001	505

28. a. 1 b. +6 c. +24 d. −27 e. −11

31. a. 11100101 b. 00000011 c. 00010101 d. 00001000 e. 11101110

32. a. 01101 b. 00000 c. 10000 (incorrect) d. 10001 e. 11110
f. 10011 (incorrect) g. 11110 h. 01101 i. 10000 (incorrect) j. 11111

33. a.

```
  5                  00101
+ 1      becomes   + 00001
                     00110   which represents 6
```

b.

```
  5                  00101                    00101
- 1      becomes   - 00001   which converts to + 11111
                                                00100 which represents 4
```

c.

```
  12                 01100                    01100
- 5      becomes   - 00101   which converts to + 11011
                                                00111   which   represents 7
```

d.

```
  8                  01000                    01000
- 7      becomes   - 00111   which converts to + 11001
                                                00001 which represents 1
```

e.

```
  12                 01100
+ 5    becomes     + 00101
                     10001     which represents -15 (overflow)
```

f.

```
  5                  00101                    00101
- 11     becomes   - 01011   which converts to + 10101
                                                11010 which represents -6
```

34. a. 3 3/4 b. 4 5/16 c. 13/16 d. 1 e. 2 1/4

35. a. 101.11 b. 1111.1111 c. 101.011 d. 1.01 e. 110.101

40. The value one-eighth, which would be represented as 00101000.

41. Since the value one-tenth cannot be represented accurately, such recordings would suffer from truncation errors.

47. 1123221343435

48. yyxy xx yyxy xyx xx xyx

49. Starting with the first entries, they would be x, y, space, xxy, yyx, and xxyy.

Chapter 2

5.

Program counter	Instruction register	Memory cell at 02
02	2211	32
04	3202	32
06	C000	11

7. a. OR the contents of register 2 with the contents of register 3 and place the result in register 1.

b. Move the contents of register E to register 1.

c. Rotate the contents of register 3 four bits to the right.
d. Compare the contents of registers 1 and 0. If the patterns are equal, jump to the instruction at address 00. Otherwise, continue with the next sequential instruction.
e. Load register B with the value (hexadecimal) CD.

9. a. 2677 b. 1677 c. BA24 d. A403 e. 81E2

17. a. 04 b. 04 c. 0E

20. The point to this problem is that a bit pattern stored in memory is subject to interpretation—it may represent part of the operand of one instruction and the op-code field of another.

a. Registers 0, 1, and 2 will contain 32, 24, and 12, respectively.

b. 12

c. 32

33.

a.	b.	c.	d.
1044	1034	10A5	10A5
30AA	21F0	210F	210F
	8001	8001	8001
	3034	12A6	4001
		21F0	A104
		8212	7001
		7002	30A5
			30A6

48. The typist would be producing characters at the rate of 4 characters per second, which translates to 32 bps (assuming each character consists of 8 bits).

50.

Address	Contents
00,01	20C1 Initialize registers.
02,03	2100
04,05	2201
06,07	130B
08,09	B312 If done, go to halt.
0A,0B	31A0 Store 00 at destination.
0C,0D	5332 Change destination
0E,0F	330B address,
10,11	B008 and go back.
12,13	C000

52. 1.74 megabits

5. Real-time operating systems are operating systems that execute the desired tasks in real time i.e., within the specified deadline. The response time of such operating systems is usually very less.

13. Virtual memory is the memory space whose presence is merely simulated by swapping blocks of data back and forth between a disk and the memory actually present in the machine.

15. If both processes merely need to read from the file, no conflicts will occur. However, if one of the processes is going to modify the file, them it should have exclusive access. (Such problems are discussed in Section 9.5 in the context of databases.)

23. At least half. This does not include the time required to actually transfer the data. 25 milliseconds = 25,000,000 nanoseconds. Thus, 250,000,000 instructions could be executed during this time.

25. The I/O-bound process. This allows the controllers to start with the I/O activities. Then the compute-bound process can run while the other is waiting for these slower activities to take place. As a general rule of thumb, priority should be given to the slower activity.

26. A mix of I/O-bound and compute-bound processes will normally produce a higher throughput than a collection of processes with similar characteristics. For example, little is gained by allowing a collection of compute-bound processes to share time. In fact, such a collection will usually get done faster without the delays caused by switching repeatedly among the different processes in the collection. However, in the case of several I/O bound processes, it could be that the relative timing of the I/O requests would produce benefits in a multiprogramming environment.

35. Our approach to the problem is to consider permission from the instructor and the payment of the fee as nonshareable resources for which the students compete.

a. This removes the competition for the nonshareable resources by removing the need for them.

b. This removes the competition for nonshareable resources by removing resources (They cannot compete because there is no resource available).

c. Here the fee payment privilege and the instructor's permission are forcibly retrieved and given to another student.

d. Here the instructor's permission is forcibly retrieved and given to the other student.

40. a. The longer a lone car waits at a red light, the higher its priority becomes. Thus, it will ultimately be given a green light at the expense of the heavier traffic.

b. The process whose time slice has just finished will most likely have the highest

priority and therefore be awarded the next time slice. This is why dynamic priority systems are used in multiprogramming systems. That is, as a process waits for a time slice, its priority increases. (In the simplest cases, processes merely wait in a queue for the next time slice. Thus a process' priority is reflected by its position in the queue. As each process completes a time slice, it is placed at the rear of the queue.)

41. It is because a malicious process can still gain access to the memory cells outside of its designated area merely by changing the special-purpose registers that contain its memory limits. That is, a process that wants to access additional memory can merely increase the value in the register containing the upper memory limit and then proceed to use the additional memory space without approval from the operating system.

42. The point of this problem is as much to introduce students to this piece of computer science folklore as it is to pose the problem itself. Issues include the problem of each philosopher obtaining possession of one fork as well as the problem of a philosopher's neighbors obtaining possession of the forks available to him and never releasing them.

47. 26^9 milliseconds, which is many years. (The point is that milliseconds add up.)

Chapter 4

6. Both the nodes will pause for a brief, independently random period of time before trying to transmit again.

16. The values 134, 48, 4, and 122 (base ten) are written 10000110, 110000, 100, and 1111010 in base two. Therefore the 32-bit address would be 8630047A in hexadecimal.

25. The Internet is a world-wide network of computer networks. The World Wide Web is a collection of hypertext documents available on the Internet.

44. It means that before any messages are exchanged between the sender and the destination, the TCP first establishes a connection between the both.

45. a. At the application layer
    b. At the network layer
    c. At the transport layer

49. Certificate authorities play a vital role in public-key encryption because they are trusted Internet sites whose task is to maintain accurate lists of parties and their public keys.