

Name\_\_\_\_\_ Student ID\_\_\_\_\_ Department/Year\_\_\_\_\_

## **Mid-term Examination**

Introduction to Computer Science  
Class#: 901 E10110, Session#: 03  
Spring 2015

15:40-17:20 Wednesday  
April 22, 2015

### **Prohibited**

1. You are not allowed to write down the answers using pencils. Use only black- or blue-inked pens.
2. You are not allowed to read books or any references not on the question sheets.
3. You are not allowed to use calculators or electronic devices in any form.
4. You are not allowed to use extra sheets of papers.
5. You are not allowed to have any oral, visual, gesture exchange about the exam questions or answers during the exam.

### **Cautions**

1. Check if you get **12** pages (including this title page), **14** questions.
2. Write your name (in Chinese), student ID, and department/year down on top of the cover page.
3. There are in total **100** points to earn. You have **100** minutes to answer the questions. Skim through all questions and start from the questions you feel more confident with.
4. You are allowed to use **English only** to answer the questions. Misspelling and grammar errors will be tolerated, but you want to make sure with those errors your answers will still make sense.
5. If you have any extra-exam emergency or problem regarding the exam questions, raise your hand quietly. The exam administrator will approach you and deal with the problem.

The following table is from Appendix C of the text. It is included here so for your reference. Questions in this exam refer to this table as the “**language description table.**”

Op-Code	Operand	Description
1	RXY	LOAD the register R with the bit pattern found in the memory cell whose address is XY. <i>Example:</i> 14A3 would cause the contents of the memory cell located at address A3 to be placed in register 4.
2	RXY	LOAD the register R with the bit pattern XY. <i>Example:</i> 20A3 would cause the value A3 to be placed in register 0.
3	RXY	STORE the bit pattern found in register R in the memory cell whose address is XY. <i>Example:</i> 35B1 would cause the contents of register 5 to be placed in the memory cell whose address is B1.
4	ORS	MOVE the bit pattern found in register R to register S. <i>Example:</i> 40A4 would cause the contents of register A to be copied into register 4.
5	RST	ADD the bit patterns in registers S and T as though they were two’s complement representations and leave the result in register R. <i>Example:</i> 5726 would cause the binary values in registers 2 and 6 to be added and the sum placed in register 7.
6	RST	ADD the bit patterns in registers S and T as though they represented values in floating-point notation and leave the floating-point result in register R. <i>Example:</i> 634E would cause the values in registers 4 and E to be added as floating-point values and the result to be placed in register 3.
7	RST	OR the bit patterns in registers S and T and place the result in register R. <i>Example:</i> 7CB4 would cause the result of ORing the contents of registers B and 4 to be placed in register C.
8	RST	AND the bit patterns in register S and T and place the result in register R. <i>Example:</i> 8045 would cause the result of ANDing the contents of registers 4 and 5 to be placed in register 0.
9	RST	EXCLUSIVE OR the bit patterns in registers S and T and place the result in register R. <i>Example:</i> 95F3 would cause the result of EXCLUSIVE ORing the contents of registers F and 3 to be placed in register 5.
A	R0X	ROTATE the bit pattern in register R one bit to the right X times. Each time place the bit that started at the low-order end at the high-order end. <i>Example:</i> A403 would cause the contents of register 4 to be rotated 3 bits to the right in a circular fashion.
B	RXY	JUMP to the instruction located in the memory cell at address XY if the bit pattern in register R is equal to the bit pattern in register number 0. Otherwise, continue with the normal sequence of execution. (The jump is implemented by copying XY into the program counter during the execute phase.) <i>Example:</i> B43C would first compare the contents of register 4 with the contents of register 0. If the two were equal, the pattern 3C would be placed in the program counter so that the next instruction executed would be the one located at that memory address. Otherwise, nothing would be done and program execution would continue in its normal sequence.
C	000	HALT execution. <i>Example:</i> C000 would cause program execution to stop.

1. Answer the following questions about binary and base-ten representation conversion (5%).

(a) What is the binary representation of  $8 \frac{5}{16}$ ?

(b) What is the base-ten representation of 111.1101?

Ans:

(a) 1000.0101

(b)  $7 \frac{13}{16}$

2. Which(s) of the following bit patterns (in hexadecimal notation) represents a positive number in two's complement notation in an 8-bit system (5%)?

(a) 00      (b) AA    (c) 88      (d) 3E

Ans:

(a)(d)

3. What decimal integer value is represented by each of the following patterns in excess notation (5%)?

(a) 11011

(b) 0000

Ans:

(a) 11

(b) -8

4. Which of the following addition problems cannot be solved accurately when using a floating-point system in which each value is encoded by a byte whose most significant bit is the sign bit, the next three bits represent the exponent field in excess notation, and the last four bits represent the mantissa (5%)?

(a)  $4 \frac{3}{4} + 3 \frac{1}{2}$

(b)  $\frac{1}{2} + \frac{1}{16}$

Ans:

(a)

5. The following is an LZ77-compressed message (5%).

ABCD (3,2,D)(4,3,D)(3,2,D)(4,3,D)(3,2,D)

- (a) How long was the original message?
- (b) Decompress the message.

Ans:

(a) 21

(b) ABCD BCD DBCD BCD DBCD BCD

6. The following is an error-correcting code in which any two patterns differ by a Hamming distance of at least three. Decode each of the following patterns (5%).

Symbol	Representation
A	000000
B	001111
C	010011
D	011100
E	100110
F	101001
G	110101
H	111010

- (a) 000000
- (b) 000011
- (c) 111000
- (d) 111111

Ans:

(a) A (b) C (c) H (d) can't be sure (B, G, or H)

7. Encode each of the following commands in terms of the machine language described in the language description table (5%).

- (a) LOAD register A with the value BC
- (b) LOAD register A with the value in memory cell BC

Ans:

- (a) 2ABC
- (b) 1ABC

8. Decode each of the following instructions based on the machine language described in the language description table (5%).

- (a) 5ABC
- (b) 6ABC

Ans:

- (a) Interpret the bit patterns in register B and C as integers and leave the resulting sum in register A
- (b) Interpret the bit patterns in register B and C as floating point numbers and leave the resulting sum in register A

9. The following table shows a portion of a machine's memory containing a program written in the language described in the language description table. Answer the questions below assuming that the machine is started with its program counter containing 05 (10%).

address	content	address	content	address	content
00	09	09	12	A3	31
01	03	0A	02	A4	54
02	01	0B	13	A5	42
03	00	0C	03	A6	B0
04	EE	0D	14	A7	A0
05	10	0E	03	A8	33
06	00	A0	B4	A9	04
07	11	A1	A8	AA	C0
08	01	A2	53	AB	00

- (a) What value (in hexadecimal notation) will be in register 4 when the machine halts?
- (b) What content (in hexadecimal notation) will be at memory location 04 when the machine halts?
- (c) If the content of memory location 01 is 04 at the first place, what will be the content (in hexadecimal notation) at memory location 04 when the machine halts?

Ans: (a) 09 (b) 1B (c) 24

10. Using the machine language described in the language description table, write a sequence of instructions that will compare the value in memory cell AA to the value in memory cell BB. If the values are the same, jump to instructions in memory cell CC (10%).

Ans:

2000

1XAA

1YBB

9ZXY

BZCC

(where X, Y, Z can be any distinct registers)



11. Suppose there is a computer system, in which the physical memory space is only 4 pages large. Suppose also that there is a process requiring 5 pages of memory space to store all data needed. Let the process start on the computer system, and the data are loaded page by page on to the physical memory in the following order: 1, 1, 2, 2, 2, 2, 3, 3, 3, 3, 1, 1, 4, 5, 4, 5.

- (a) Which data pages are swapped out subsequently if the computer system's swapping policy is Oldest First (5%)?
- (b) Which data pages are swapped out subsequently if the computer system's swapping policy is Least (Frequently) Used (5%)?
- (c) Which data pages are swapped out subsequently if the computer system's swapping policy is Least Recently Used (5%)?

Ans:

(a)

1, 1, 2, 2, 2, 2, 3, 3, 3, 3, 1, 1, 4, 5, 4, 5

- , - , - , - ,   - , - , - , - ,   - , - , - , - ,   - , 1, - , -

(b)

1, 1, 2, 2, 2, 2, 3, 3, 3, 3, 1, 1, 4, 5, 4, 5

- , - , - , - ,   - , - , - , - ,   - , - , - , - ,   - , 4, 5, 4

(c)

1, 1, 2, 2, 2, 2, 3, 3, 3, 3, 1, 1, 4, 5, 4, 5

- , - , - , - ,   - , - , - , - ,   - , - , - , - ,   - , 2, - , -

12. What is a timesharing system (5%)?

Ans:

- In a timesharing system, the CPU time is divided into time slices
- Only one process runs on the CPU at any time slice.
- Multiple processes/jobs can switch turns running on the CPU one time slice at a time.
- The time slice is so small that, the user does not perceive the switching, and thus creating the illusion that the system supports the execution of multiple processes/jobs simultaneously.

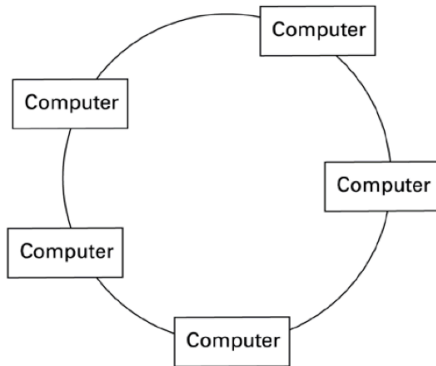
13. Describe a scenario that leads to a deadlock in real life. Please specify the processes and the resources they compete for (10%).

Ans:

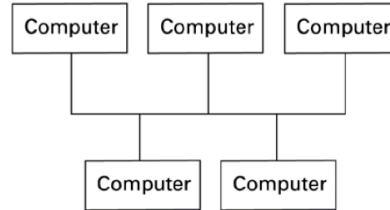
There are many possible answers. It involves generally two entities, each of which needs additional resources to complete its task that is occupied by the other entity. The resource must be non-sharable.

14. Consider the following 4 network topologies.

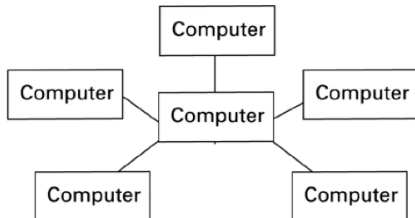
(1)



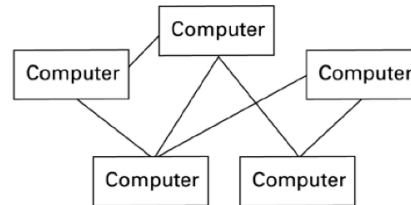
(2)



(3)



(4)



(a) Which is a star, which is a ring, and which is a bus topology accordingly (5%)?

(b) Which is more likely the construct of a WAN, and why (5%)?

Ans:

(a) (3) (1) (2)

(b) (4), WAN is a composition of many smaller networks and each of these smaller networks can be in different network topology. The resulting big network is therefore often irregular like the one shown in (4).