Introduction to
Semiconductor Processing

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晶圓準備

- CMOS IC 晶片通常使用 <100> 晶圓
- 二極體和BiCMOS 晶片通常使用 <111> 晶圓
- 1960 到1970年代中葉，大部分使用PMOS，N型晶圓
- 1970中葉以後，主要以 NMOS，P型晶圓
- CMOS 從 NMOS製程發展而得，主要因大部分廠原先皆使用P型晶圓

2

磊晶矽層

- 高速CMOS晶片需磊晶層
- 由CZ法所得之矽晶圓皆含有部分氧原子，其係源自石英坩堝
- 氧原子會縮短載子生命週期並減緩元件速度
- 矽磊晶層創造一無氧之基片並幫助達到高元件速率
- 先進的CMOS IC晶片通常使用具P型磊晶層之 p型 <100> 單晶矽晶圓
- 雙極體(bipolar) IC晶片通常使用 <111> 晶圓

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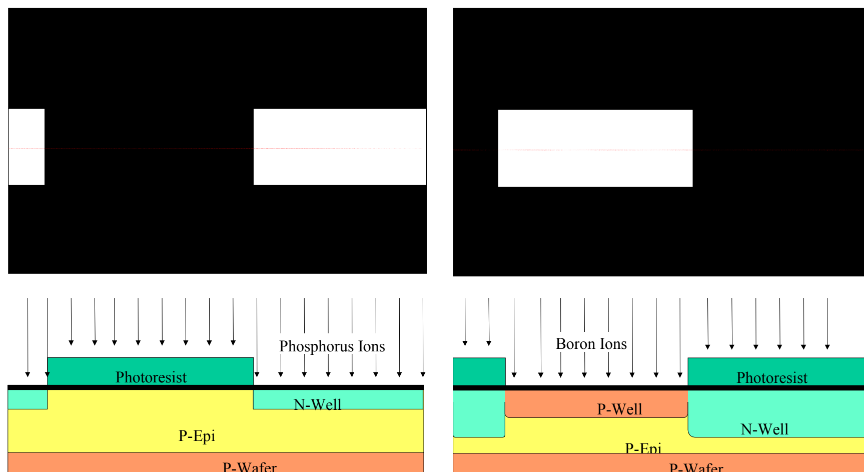
Twin Well



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淺溝槽絕緣 (STI)

- LOCOS 和 PBL 運作地很好當圖形尺寸 > 0.5 μm 時
- 當圖形尺寸 < 0.35 μm爲不能容忍的
- 矽蝕刻及淺溝槽的氧化 被研究來減少氧化物侵入
- STI製程和CVD氧化物溝槽之填充被接著發展出來

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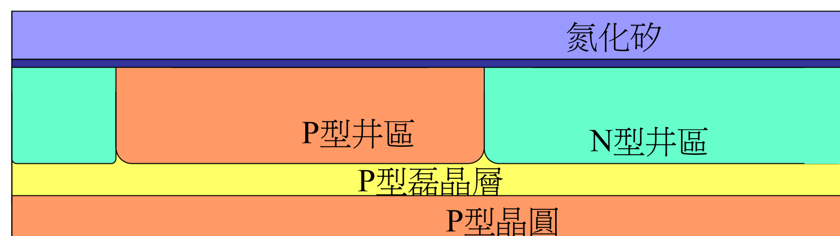
STI: 襯墊氧化及 LPCVD 氮化矽



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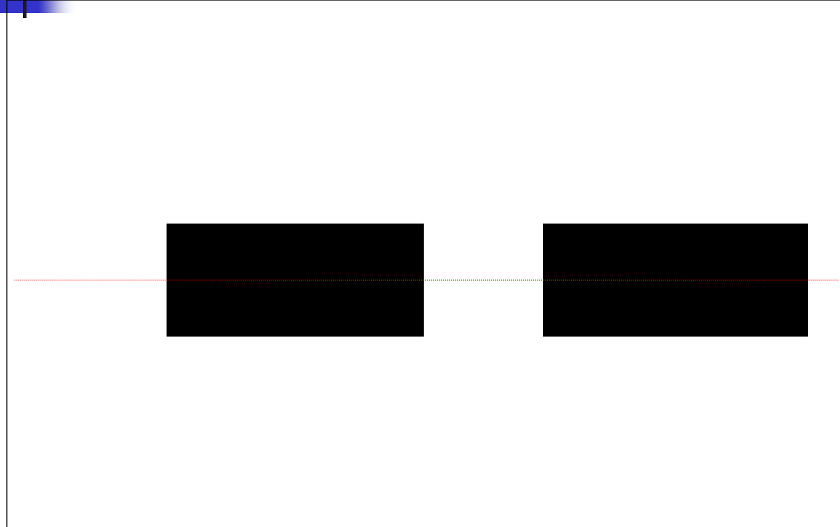
STI: STI光罩



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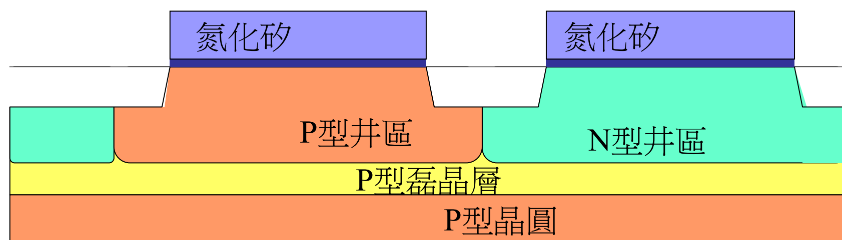
STI: 氮化矽、氧化矽及矽之蝕刻，光阻剝除



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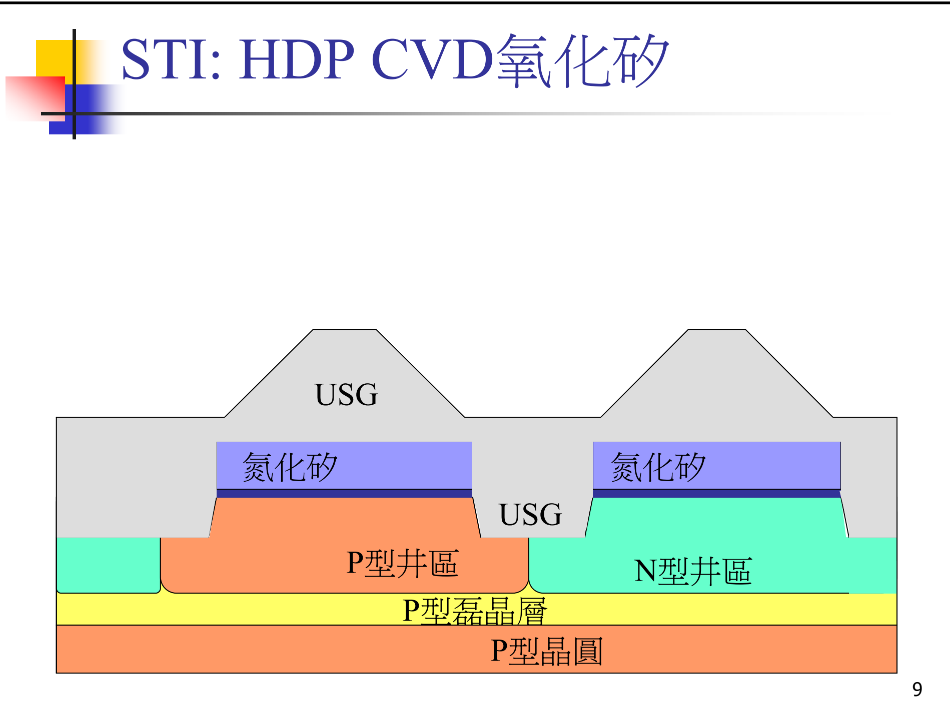
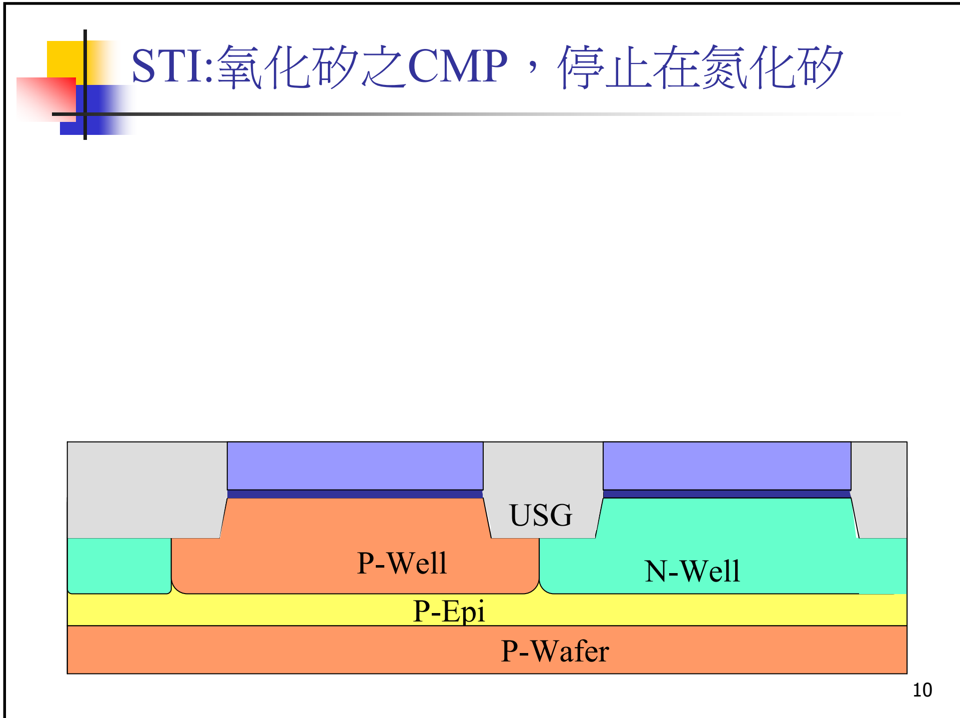
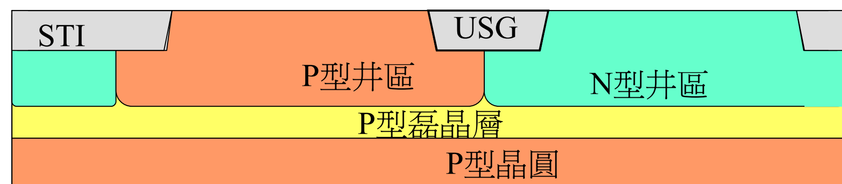

STI: HDP CVD氧化矽
USG
氮化矽
氮化矽
USG
P型井區
N型井區
P型磊晶層
P型晶圓
9


STI:氧化矽之CMP，停止在氮化矽
USG
P-Well
N-Well
P-Epi
P-Wafer
10

STI: 氮化矽剝除



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自我對準閘極

- 離子佈值介紹
- NMOS取代PMOS
- 閘極材料由多晶矽取代鋁
  - 鋁合金不能在佈植後高溫退火中維持

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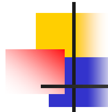
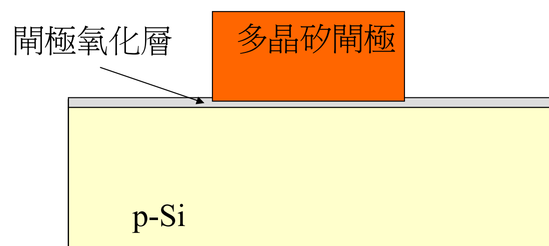


多晶矽蝕刻, 光阻剝除及多晶矽退火



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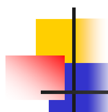
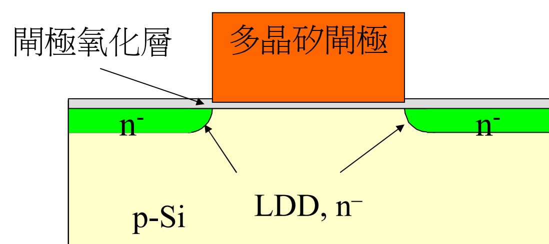


LDD佈植



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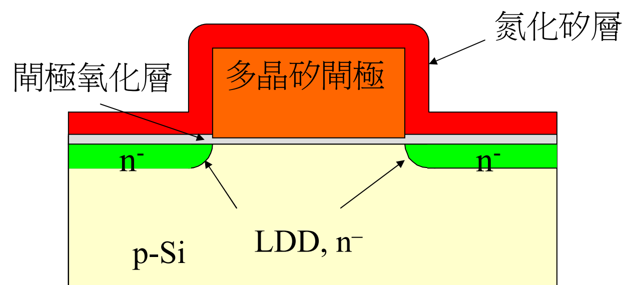
氮化矽沈積



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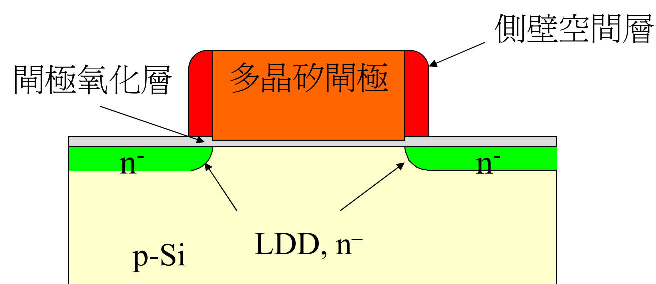
氮化矽回蝕刻



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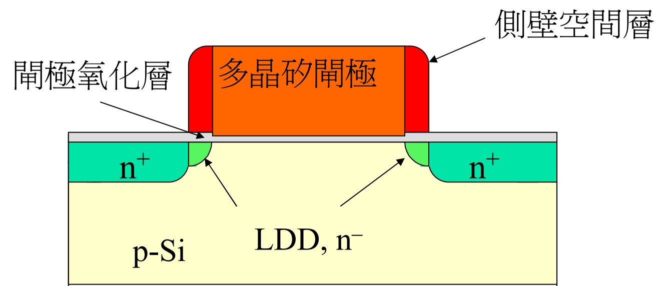
源極、汲極佈植



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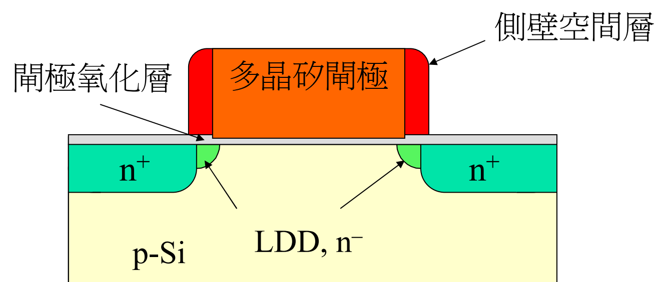
佈植退火



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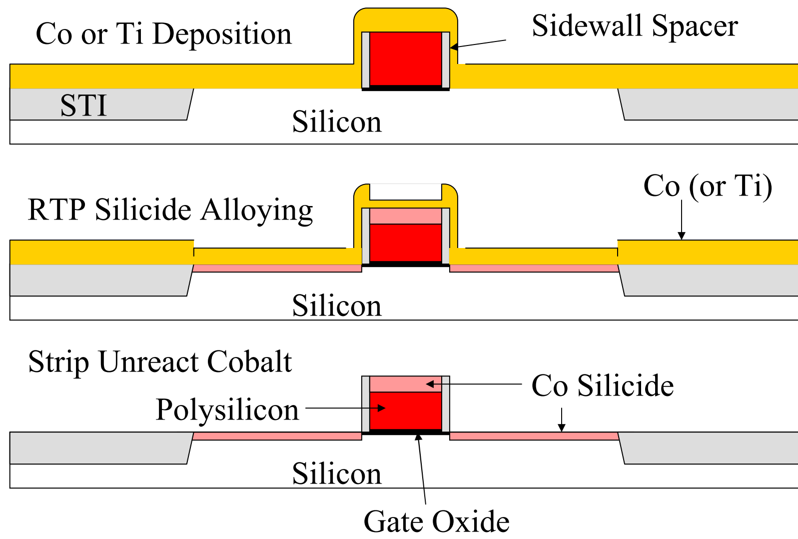
導線: Cobalt Silicide Process



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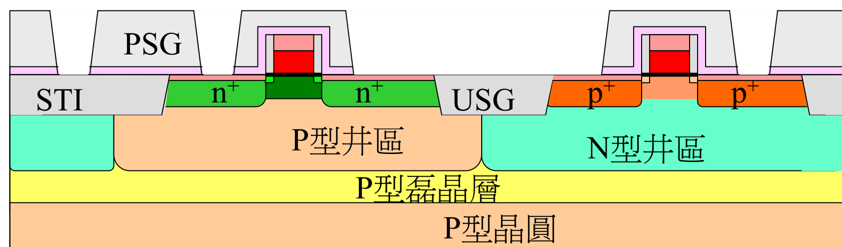
導線



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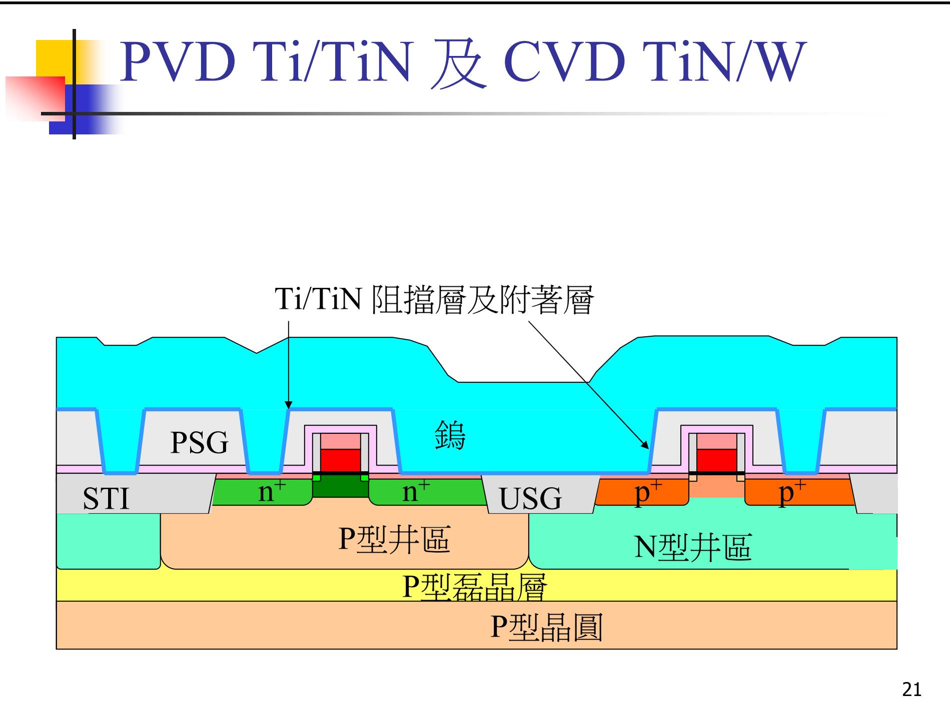
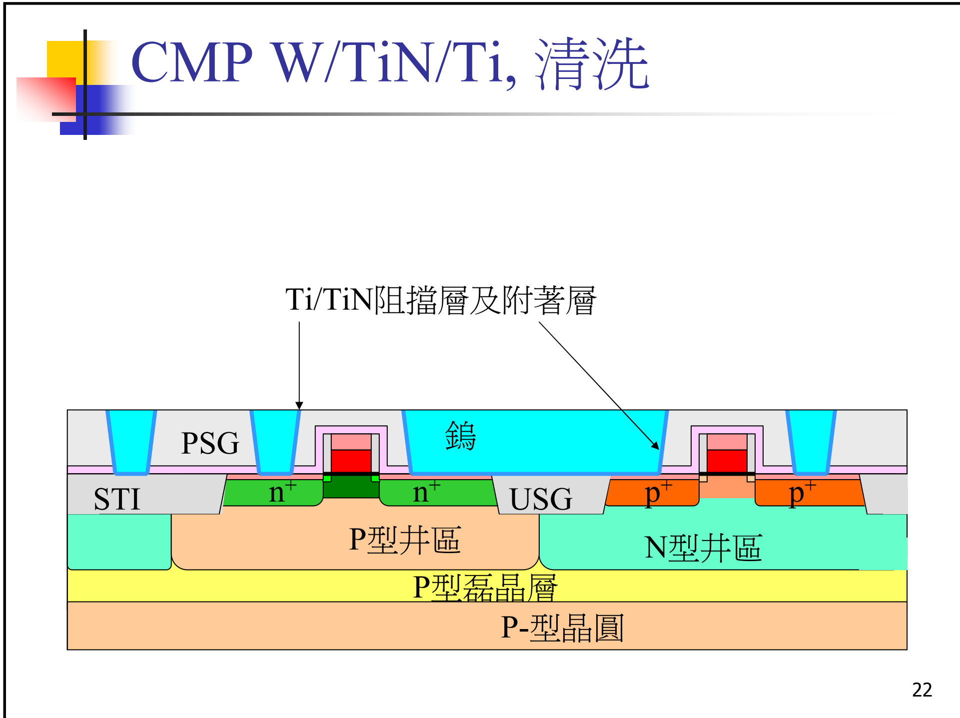
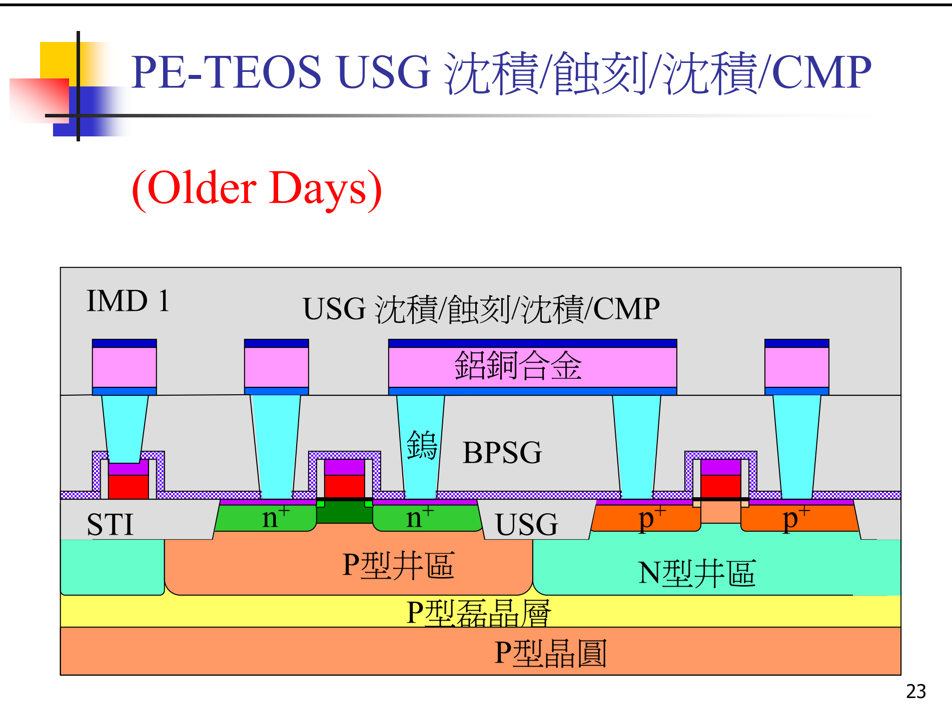
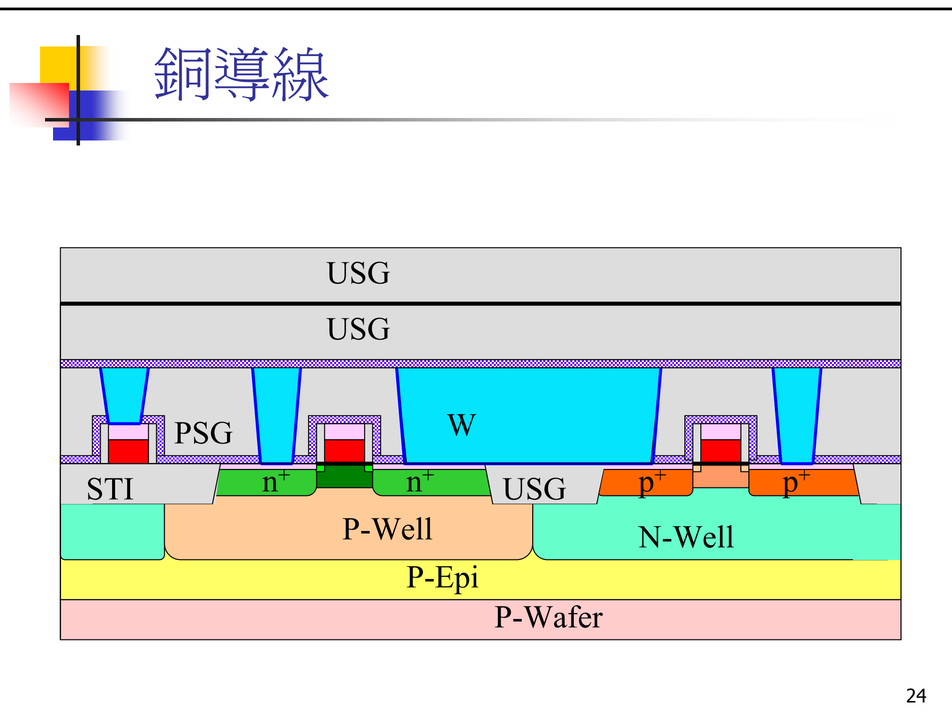

PVD Ti/TiN 及 CVD TiN/W
Ti/TiN 阻擋層及附著層
PSG
鎢
STI
n+
n+
USG
p+
p+
P型井區
N型井區
P型磊晶層
P型晶圓
21


CMP W/TiN/Ti, 清洗
Ti/TiN阻擋層及附著層
PSG
鎢
STI
n+
n+
USG
p+
p+
P型井區
N型井區
P型磊晶層
P-型晶圓
22


PE-TEOS USG 沈積/蝕刻/沈積/CMP
(Older Days)
IMD 1
USG 沈積/蝕刻/沈積/CMP
鋁銅合金
鎢
BPSG
STI
n+
n+
USG
p+
p+
P型井區
N型井區
P型磊晶層
P型晶圓
23


銅導線
USG
USG
PSG
W
STI
n+
n+
USG
p+
p+
P-Well
N-Well
P-Epi
P-Wafer
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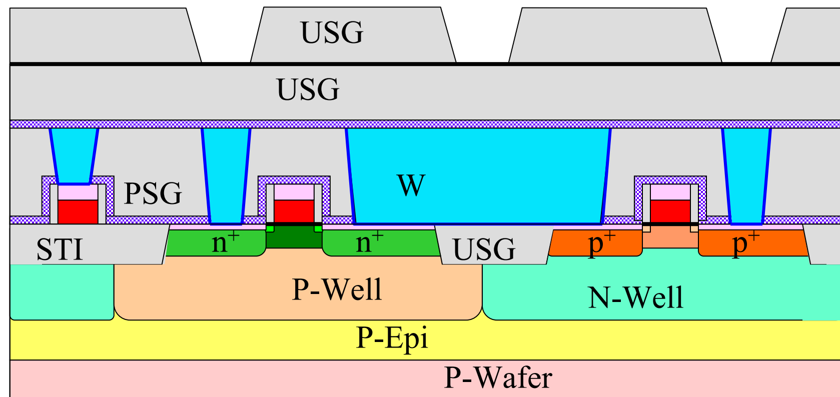
Via Mask, Etch Via, and Strip PR



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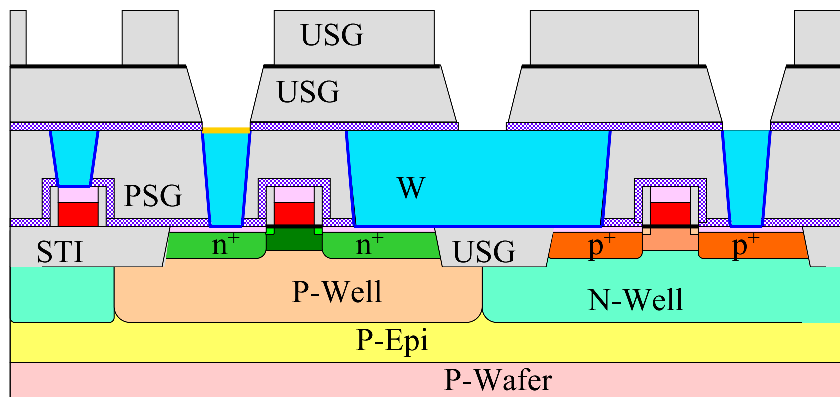
Trench Mask, Etch Trench, Strip PR



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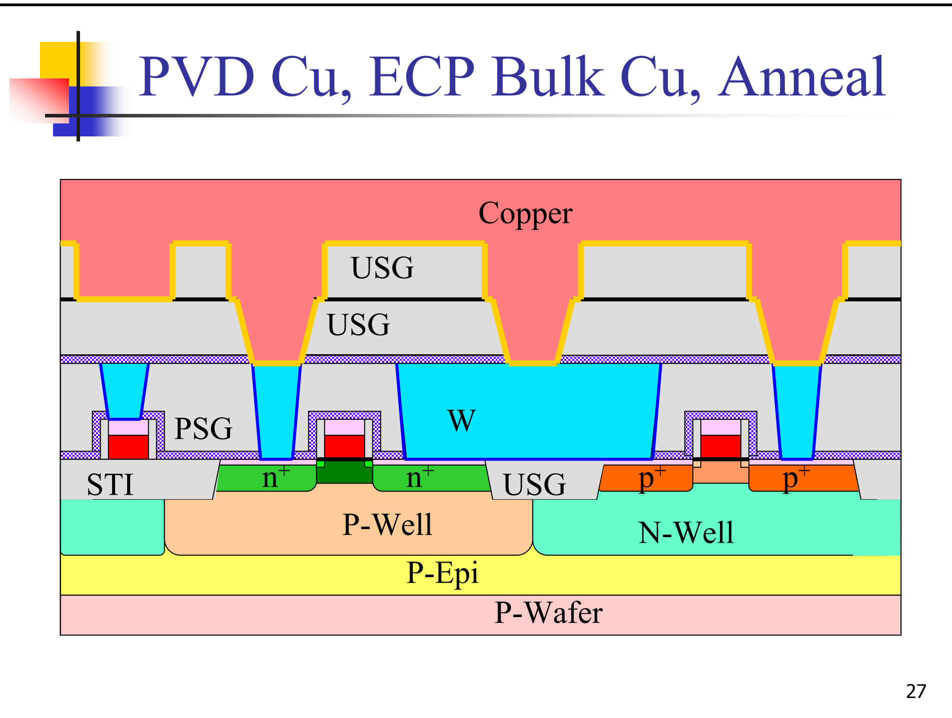
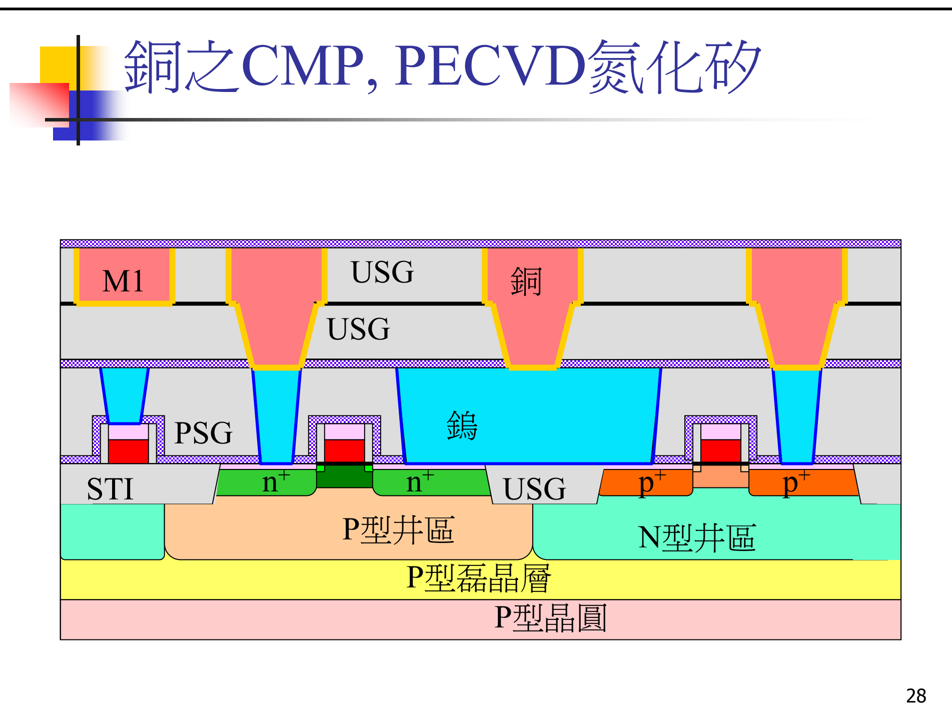

PVD Cu, ECP Bulk Cu, Anneal
Copper
USG
USG
PSG
W
STI
n+
n+
USG
p+
p+
P-Well
N-Well
P-Epi
P-Wafer
27


銅之CMP, PECVD氮化矽
M1
USG
銅
USG
PSG
鎢
STI
n+
n+
USG
p+
p+
P型井區
N型井區
P型磊晶層
P型晶圓
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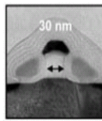
Look Beyond: Challenges and Opportunities

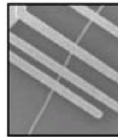
What Experts Said:

- "I think there is a world market for about five computers." – Thomas Watson (the President of IBM), 1943
- "640k ought to be enough for anybody." – Bill Gates, 1981
- **"There is Plenty of Room at the Bottom." – Richard Feynman, 1959**

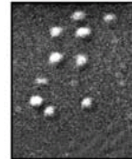


High k
Metal Gate

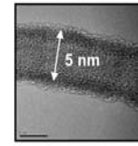
Innovations beyond Imaginations



Carbon
Nanotube



Quantum Dots



Nanowire

C. R. Barrett, MRS Bulletin, 31, 906 (2006)

Beyond Current Transistors

2007 ***2011*** ***2015***

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