Ch10 Chemical Vapor Deposition and Dielectric

Introduction to
Semiconductor Processing

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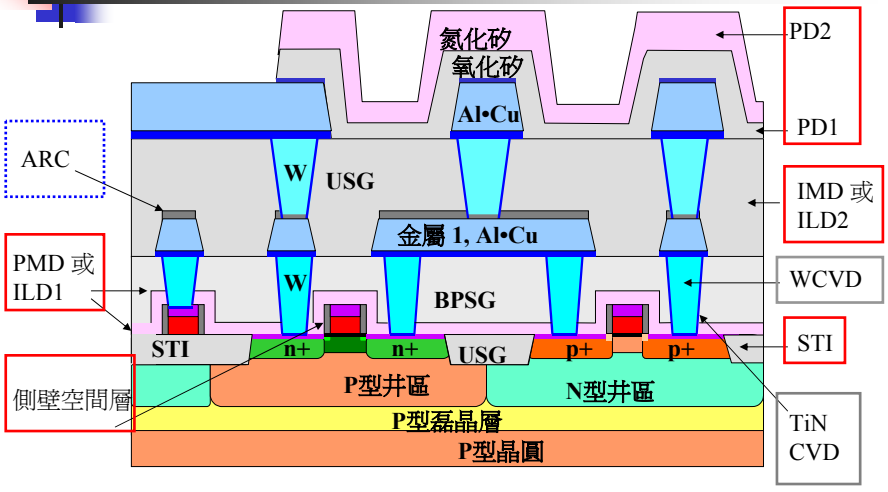
Dielectric Layers



ARC: 反射層鍍膜;
PMD: 金屬沈積前的介電質層;
LDD: 低摻雜汲極;

IMD: 屬層間介電質層;
STI: 淺溝槽絕緣;
ILD:金屬層間介電質層

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CVD 應用

	薄膜	*先驅物*
半導體	Si (poly) Si (epi)	SiH_4 (silane) $SiCl_2H_2$ (DCS) $SiCl_3H$ (TCS) $SiCl_4$ (Siltet)
介電質	SiO_2 (glass)	LPCVD SiH_4, O_2 PECVD SiH_4, N_2O PECVD $Si(OC_2H_5)_4$ (TEOS), O_2 LPCVD TEOS APCVD&SACVD™ TEOS, O_3 (ozone)
	Oxynitride	SiH_4, N_2O, N_2, NH_3
	Si_3N_4	PECVD SiH_4, N_2, NH_3 LPCVD SiH_4, N_2, NH_3 LPCVD $C_8H_{22}N_2Si$ (BTBAS)
導體	W (Tungsten) WSi_2 TiN Ti Cu	WF_6 (Tungsten hexafluoride), SiH_4, H_2 WF_6 (Tungsten hexafluoride), SiH_4, H_2 $Ti[N(CH_3)_2]_4$ (TDMAT) $TiCl_4$

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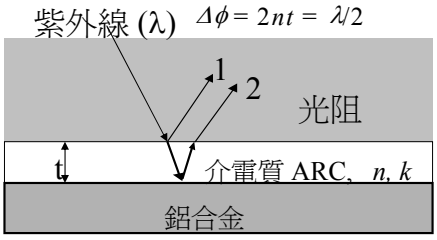
介電質抗反射層鍍膜 (ARC)



ARC: Anti-reflection Coating

Reflectivity

Metal: very high

TiN: 30~40%

- W/O ARC: reflective light changes the PR light exposure
- W/ ARC: destructive interference eliminates the reflection light
- By well adjusting:

_____and _____

Reflective light can be fully eliminated

- Essential for 0.25 μm and beyond processes

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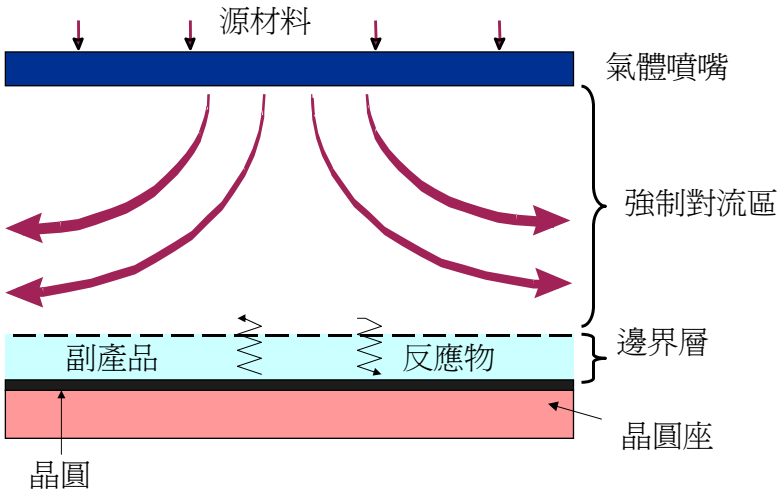
Macroscopic Transport



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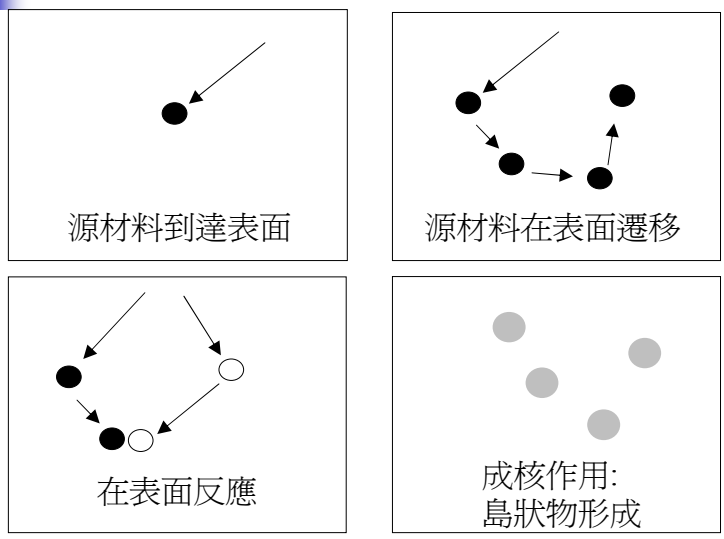
沈積製程(複晶型材料)



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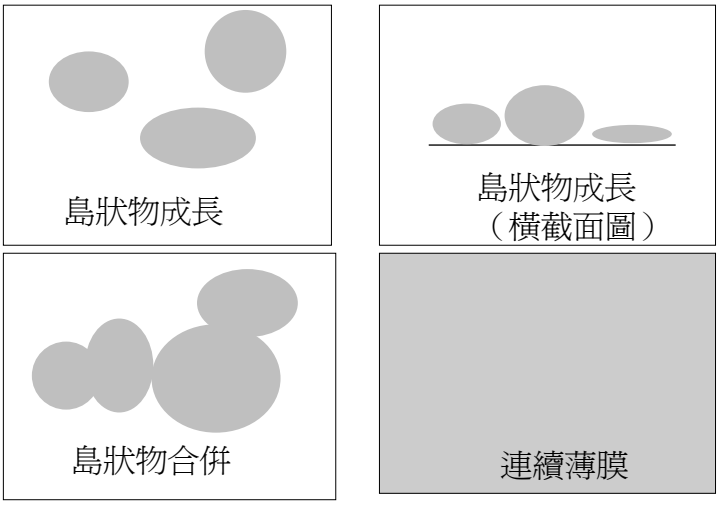
沈積製程



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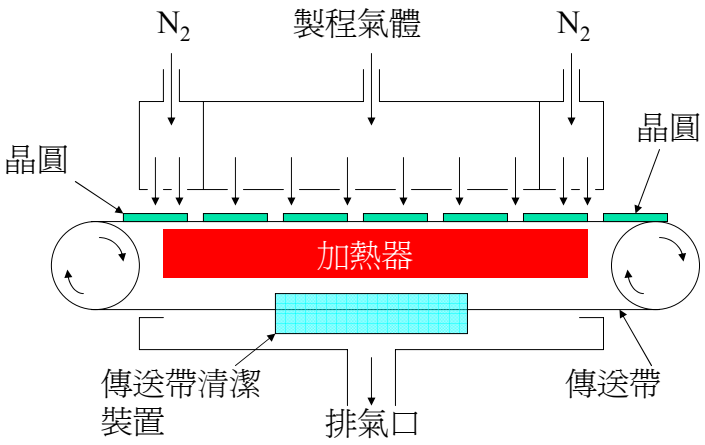
常壓 CVD (APCVD)



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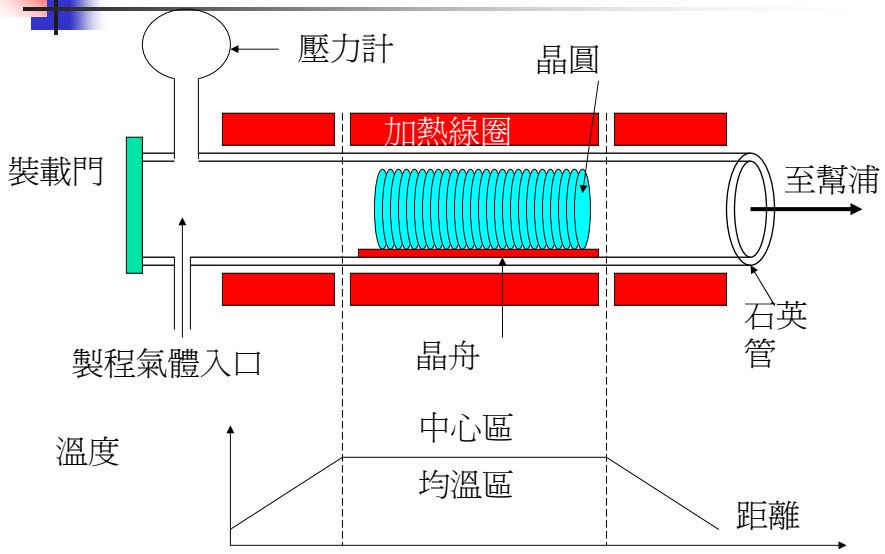
LPCVD 系統



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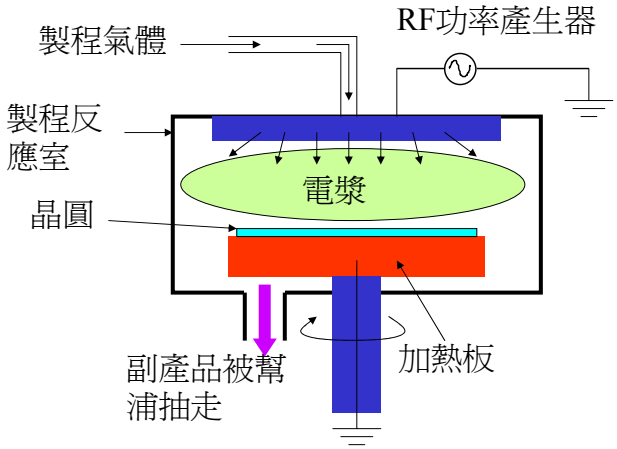
電漿增強型 CVD 系統 (PECVD)



Major Features:
1.
2.

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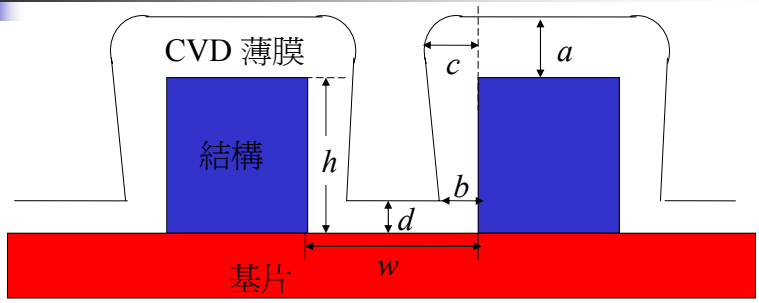
階梯覆蓋與似型性



側壁階梯覆蓋(Sidewall step coverage) = _____

底部階梯覆蓋 (Bottom step coverage)= _____

似型性 (conformality) = _____

懸凸(Overhang) = _____ (due to arriving angle of precursor)

深寬比(Aspect ratio) = _____

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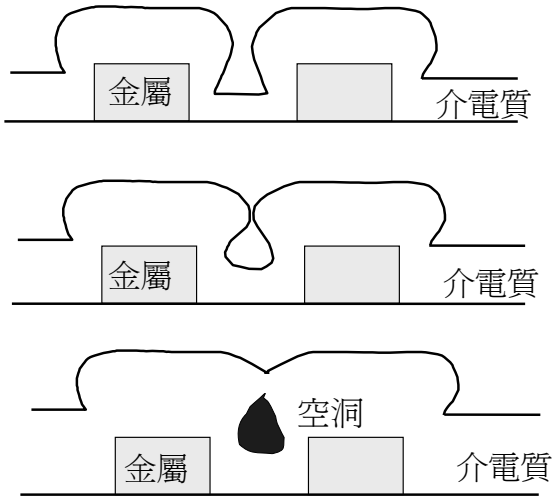
空洞形成步驟



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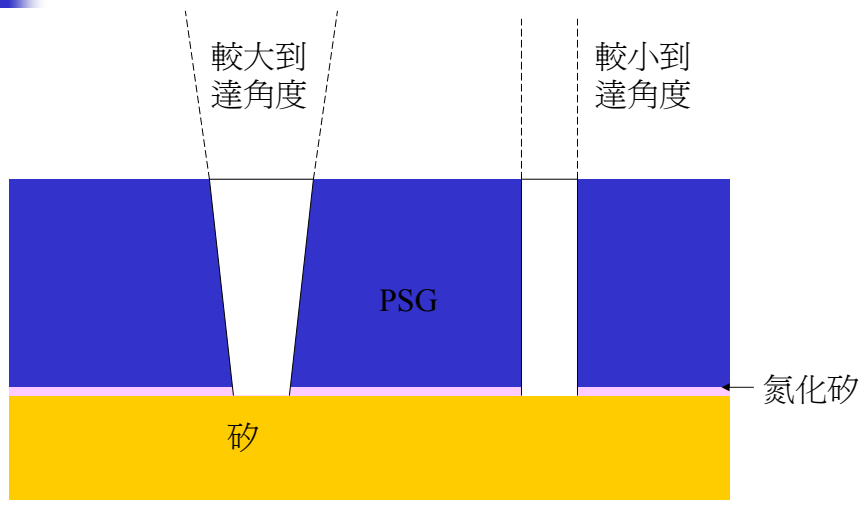
到達角度與接觸窗孔



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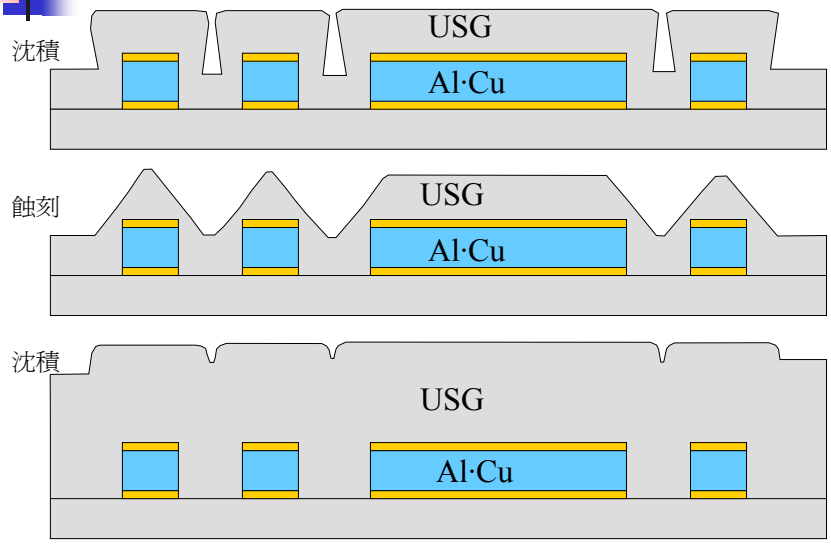
沈積/蝕刻/沈積



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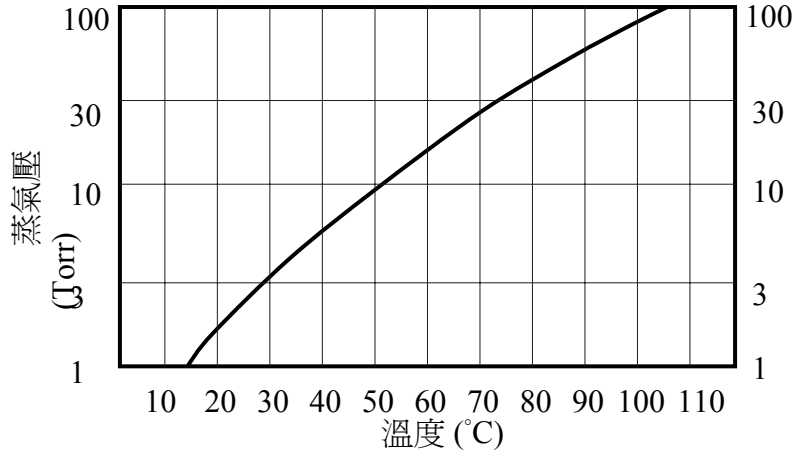
介電質 CVD 先驅物

- 矽烷 (SiH_4) → explosive and large amount of Si particles
- TEOS (四乙氧基矽烷, $Si(OC_2H_5)_4$)



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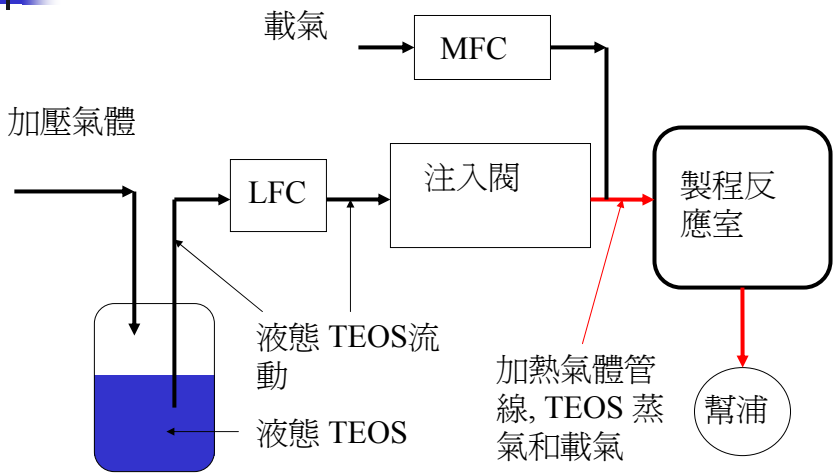
注入系統



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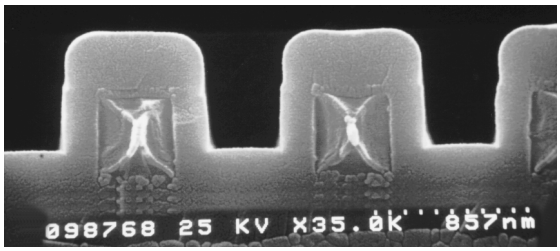
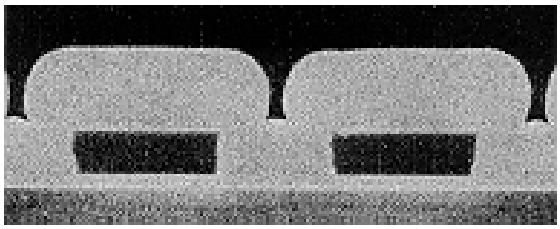
TEOS及矽烷之階梯覆蓋



TEOS



矽烷

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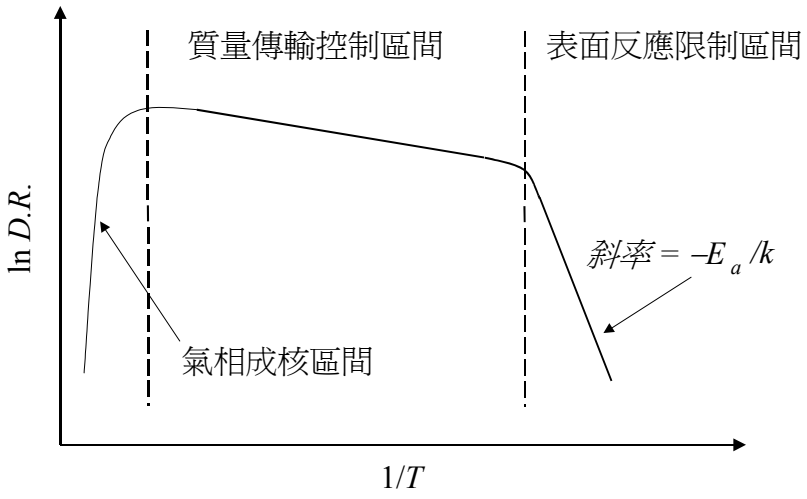
沈積速率區間



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Dielectric CVD: 氧化矽及氮化矽

氧化物 (SiO_2)	氮化物 (Si_3N_4)
高介電強度 > 1×10^7 V/cm	高介電強度 > 1×10^7 V/cm
低介電常數, $\kappa = 3.9$	較高介電常數, $\kappa = 7.0$
對濕氣及移動離子並非好的阻障層 (Na^0)	對濕氣及移動離子是好的阻障層 (Na^+)
UV可穿透	一般氮化物對UV不透明
可摻雜 P 或 B	

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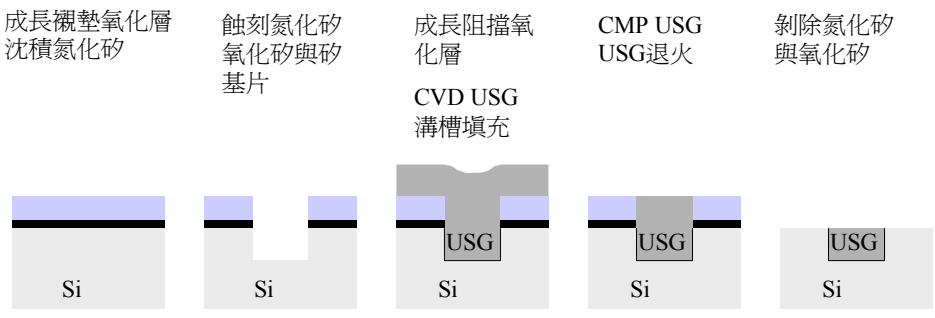
淺溝槽絕緣 (STI)



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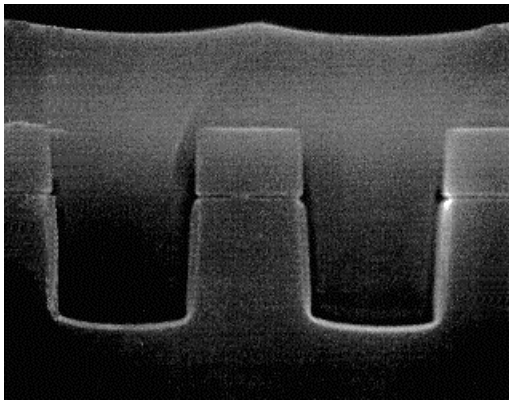
淺溝槽絕緣 (STI)



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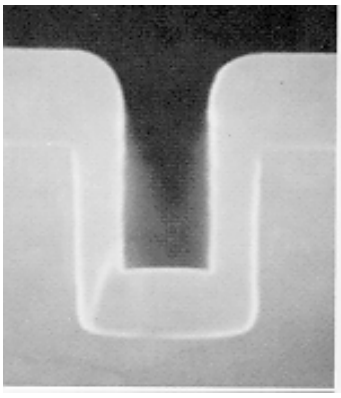
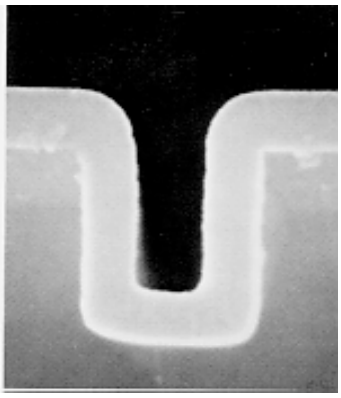
O_3-TEOS vs PE-TEOS

PE-TEOS



階梯覆蓋: 50%
似型性: 87.5%

Ozone-TEOS



階梯覆蓋: 90%
似型性: 100%

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應力

- 不同材料間的不匹配
- 兩種不同的應力, 本質(intrinsic)與異質(extrinsic)應力
- 本質應力是在薄膜成核與成長製程期間產生的
- 異質應力是因爲薄膜與基片間的熱膨脹係數不同所造成
- 張力 (tensile): 極高時產生薄膜破裂
- 收縮力 (compressive): 極高時出現金屬線尖凸現象

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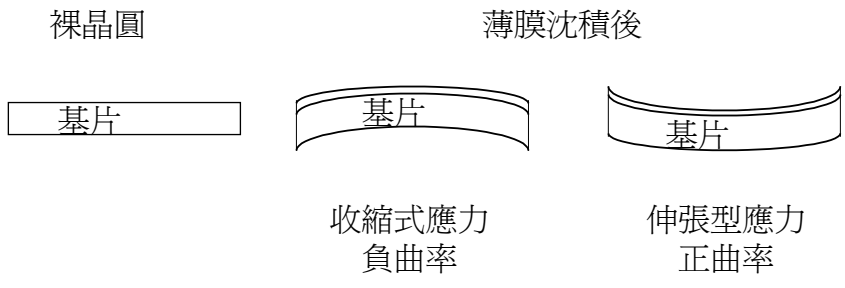
膜應力



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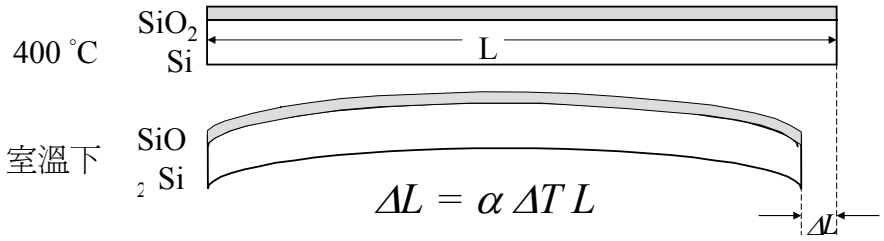
熱應力與熱膨脹係數



$\alpha(SiO_2) = 0.5\times10^{-6}\ ^\circ C^{-1}$
$\alpha(Si) = 2.5\times10^{-6}\ ^\circ C^{-1}$
$\alpha(Si_3N_4) = 2.8\times10^{-6}\ ^\circ C^{-1}$
$\alpha(W) = 4.5\times10^{-6}\ ^\circ C^{-1}$
$\alpha(Al) = 23.2\times10^{-6}\ ^\circ C^{-1}$

Oxide:

Metal:

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阻擋層: 氮化矽

- 濕氣及移動離子的阻擋層
- PECVD 氮化物
  - 低沈積溫度 (<450ºC)
  - 高沈積速率
  - 矽烷、氨氣及氮氣

$$SiH_4 + N_2 + NH_3 \xrightarrow[\text{加熱}]{\text{電漿}} SiN_xH_y + H_2 + N_2 + NH_3 + \ldots$$

- 需要好的階梯覆蓋、高沈積速率、良好的似型性及應力控制

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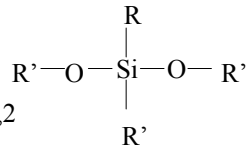
自旋塗佈矽玻璃 (SOG)

- 和光阻塗佈及烘烤製程類似
- 製造業人們喜歡熟悉的技術
- IMD 間隙填充及平坦化
- 兩種自旋塗佈玻璃:
  - 矽酸鹽
  - 矽氧烷

$R_nSi(OH)_{4-n}$, n =1,2

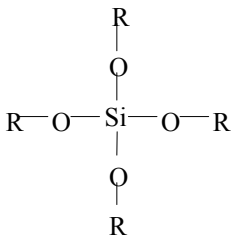
矽氧烷



$R = CH_3$,
R' = R or OH

$Si(OR)_4$

矽酸鹽



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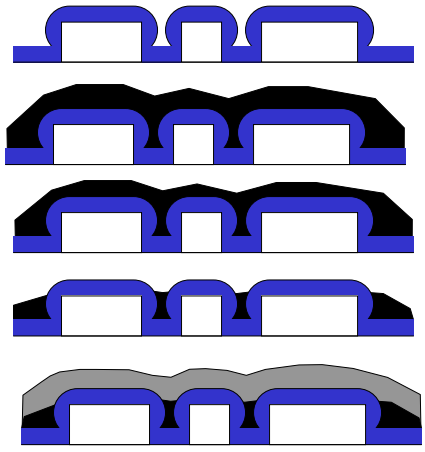
自旋塗佈矽玻璃 製程步驟



PECVD USG
阻擋層

自旋塗佈矽
玻璃

SOG 固化

SOG 回蝕刻

PECVD USG
覆蓋層

SOG:
Major advantage:

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未來趨勢: 低-κ 介電質

- 必須減少RC延遲
  - 低-κ減少*C* 且銅減少*R*
- 需高的熱穩定性、高的熱傳導性及製程整合能力
  - **CVD**
    - **CSG (C_xSi_yO, κ ~ 2.5 - 3.0) 和 α-CF (C_xF_y, κ ~ 2.5 – 2.7)**
  - **自旋塗佈介電質 (SOD)**
    - **氫矽酸鹽類 (HSQ, κ ~ 3.0), Problem:**
    - **多孔的SOD ，如乾凝膠 (κ ~ 2.0 - 2.5), Problem:**

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