

Silicon Photonics

矽光子學

Fabrication of Silicon Waveguide Devices (A)

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Outline

- 5.1 SILICON-ON-INSULATOR (SOI)
- 5.2 FABRICATION OF SURFACE ETCHED FEATURES

5.1 SILICON-ON-INSULATOR (SOI)

SILICON-ON-INSULATOR (SOI)

- SOI: a generic term used to describe structures which consist of a thin layer of crystalline silicon on an insulating layer.
- In microelectronics and photonics:
SOI \Rightarrow silicon on silicon dioxide

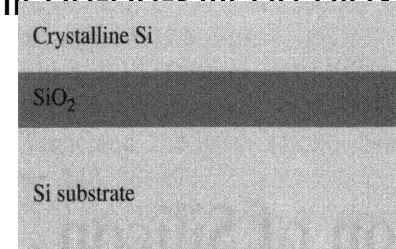


Figure 5.1 Silicon-on-silicon dioxide

Separation by IMplanted OXYgen (SIMOX)

- SIMOX process \Rightarrow the most popular method for the fabrication of large volumes of SOI material.
- Although the process is simple in concept, there exists a relatively small process window for the production of device-grade SOI.
- The key to the fabrication of SOI by the SIMOX method is the implantation of a large number of oxygen ions (controlled by the implanted ion dose) below the surface of a silicon wafer.
 - Implanted ion dose: the total number of ions that pass through one square centimeter of the wafer surface (ions/cm²)

Separation by IMplanted OXYgen (SIMOX)

- The total implantation dose required in the SIMOX process is usually $> 10^{18}$ cm⁻²
 - Compared to CMOS IC fabrication process \Rightarrow *p*- or *n*-doping: Usually 10^{16} cm⁻² for low resistance
- Under normal room-temperature conditions
 - an unwanted amorphous silicon overlayer would form during the implantation of the oxygen ions.
 - To prevent this, the silicon substrate is maintained at a temperature of approximately 600°C during implantation.

Separation by IMplanted OXYgen (SIMOX)

- Oxygen ions are implanted into crystalline silicon at an energy of up to 200 keV.
 - This energy subsequently determines the depth of the SiO₂ and hence the thickness of the silicon overlayer
- At low doses $\ll 10^{16}$ cm⁻²
 - \Rightarrow \approx gaussian function (Figure 5.2a).
- As the dose increases, the peak concentration of oxygen ions (O⁺) saturates to a concentration of that found in stoichiometric SiO₂ (Figure 5.2b).
- With further implantation (dose $> 10^{18}$ cm⁻²), the oxygen profile begins to flatten, forming a buried, continuous layer of SiO₂.

Separation by IMplanted OXYgen (SIMOX)

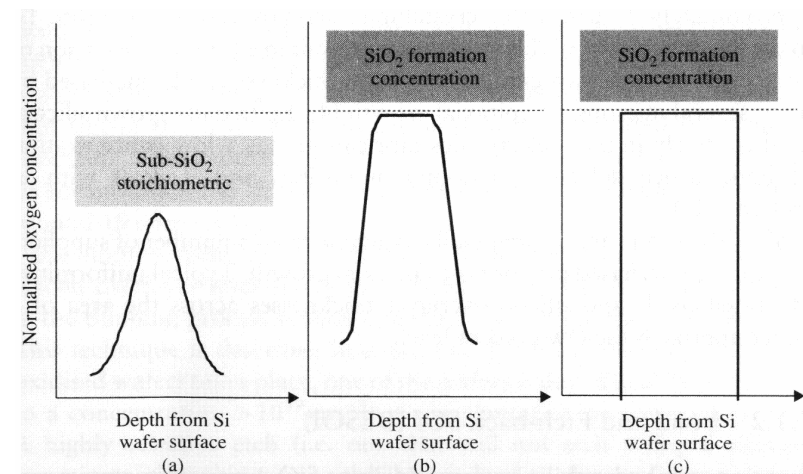


Figure 5.2 Variation of the oxygen profile during the SIMOX process. (a) Low-dose; (b) high-dose (peak is at the stoichiometric limit for SiO₂); and (c) after implantation and annealing at 1300 °C for several hours

Separation by IMplanted OXYgen (SIMOX)

- The silicon wafer is then annealed at a temperature of approximately 1300 °C for several hours.
 - This anneal produces a uniform, buried SiO₂ layer with distinct interfaces with the two adjacent silicon layers.
 - The annealing ensures the silicon overlayer is denuded of implantation-related, primary lattice defects. (Figure 5.2c)

Separation by IMplanted OXYgen (SIMOX)

- Of importance to silicon photonics is the concentration of secondary defects in the silicon overlayer (e.g., crystal dislocations), and the micro-roughness of the silicon over-layer surface and the overlayer/buried oxide interface.
- In the 1980s, the concentration of dislocations in SIMOX was approximately 10¹⁰ cm⁻².
- It is then reduced to 10² -10³ cm⁻², by optimizing fabrication conditions such as implantation substrate temperature and post-implantation annealing conditions.

Separation by IMplanted OXYgen (SIMOX)

- The depth and thickness of the buried SiO₂ layer is a function of the implant energy.
 - For a 200 keV implant the buried SiO₂ thickness is approximately 0.5 μm with a crystalline silicon overlayer of 0.3 μm.
- To make the dimensions of this structure more suitable for the fabrication of large cross-section waveguides, the silicon thickness can be increased by up to several microns via epitaxial growth.
- Epitaxially grown silicon, used routinely in microelectronics fabrication, has a low concentration of both lattice defects and doping impurities.
- SIMOX wafers are commercially available from a number of suppliers and can be purchased pre- or post-epitaxial growth.
- Typical uniformities of buried oxide and silicon overlayer thicknesses across the area of a wafer approach the few percent level.

Bond and Etch-back SOI (BESOI)

- Bringing two hydrophilic surfaces (such as SiO₂) into intimate contact can result in the formation of a very strong bond.
- The production of BESOI has three steps shown schematically in Figure 5.3:
 - (a) Oxidation of the two wafers to be bonded;
 - (b) Formation of the chemical bond;
 - (c) Thinning (etching) of one of the wafers.

Bond and Etch-back SOI (BESOI)

■ Bond

- The wafers are brought into contact at room temperature, at which point an initial bond is formed. The bond strength is increased to that of bulk material via subsequent thermal processing to temperatures as high as 1100 °C

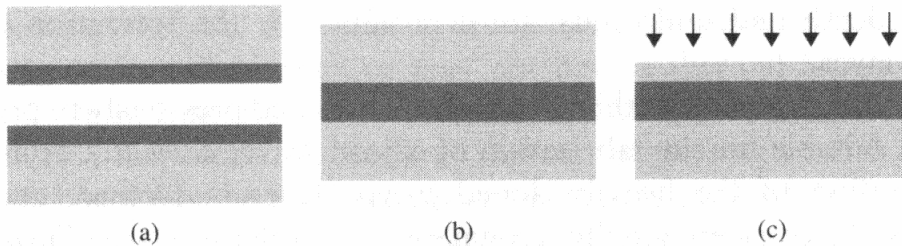


Figure 5.3 The bond and etch-back process to form BESOI: (a) oxidation; (b) bonding; and (c) thinning

Bond and Etch-back SOI (BESOI)

■ Wafer Thinning (Etching)

- *Chemical mechanical polishing (CMP)*: a technique used extensively in microelectronics for wafer planarization. CMP requires that the wafer surface be both weakened and subsequently removed during a single processing step.
 - In general, the silicon surface to be polished is brought into contact with a rotating pad, and simultaneously a chemically reactive slurry containing an abrasive component such as alumina and glycerine weakens and removes surface layers.
 - The process removes the majority of one of the bonded wafers, leaving a thin silicon overlayer on a buried SiO₂ layer, supported by a silicon substrate.
 - The rather crude method of removing hundreds of microns of silicon limits the thicknesses achievable for the silicon overlayer to around 10 microns.

Bond and Etch-back SOI (BESOI)

- An improvement in SOI thickness uniformity (and hence reduced silicon overlayer thickness) can be achieved by the use of an **End-Stop** in the thinning process reducing or even eliminating the need for CMP.
 - Before bonding of the two oxidized wafers takes place, one of the wafers is doped heavily *p-type* (i.e. to a concentration > 10¹⁹ cm⁻³) via implantation or epitaxial growth.
 - A highly selective etch (i.e. one that will not etch *p-doped* silicon), sometimes in combination with CMP, is used to remove the majority of the wafer with the *p-type* doped layer.
 - As the doped region is exposed to the etchant the etching process ceases, leaving a silicon overlayer whose depth and uniformity are determined by the formation of the doped layer.

Bond and Etch-back SOI (BESOI)

- A modified version of the **End-Stop** process has been used previously to produce wafers suitable for the fabrication of silicon waveguides.
 - Following the creation of the heavily doped *p-type* layer, a further, undoped intrinsic layer is epitaxially grown on the wafer surface.
 - Further, a second nonselective etch process is used to remove the exposed *p-type* layer following the selective etch.
 - The final wafer structure is then one of an undoped silicon overlayer on the buried SiO₂.
 - As we have seen in Chapter 4, section 4.6.2, silicon waveguides require doping levels <10¹⁶ cm⁻³, so the etch-stop consisting of dopant at a concentration > 10¹⁹ cm⁻³ must be removed from the wafer structure if the end-stop technique is to be used.

Wafer Splitting (SmartCut® Process to Produce Unibond® Wafers)

■ Smart Cut

- A thermally oxidized wafer is implanted with hydrogen to a dose of approximately 10^{17} cm⁻².
- The implanted hydrogen ions form a gaussian-like profile.
- The distance from the wafer surface of the peak of the profile depends on the H⁺ ion energy, but is usually between a few hundred nanometers and a few microns.
- The H⁺ ions, and the silicon lattice damage caused by the stopping of the ions, are at their greatest concentration at this depth, and here the silicon lattice bonds are significantly weakened.

Wafer Splitting (SmartCut® Process to Produce Unibond® Wafers)

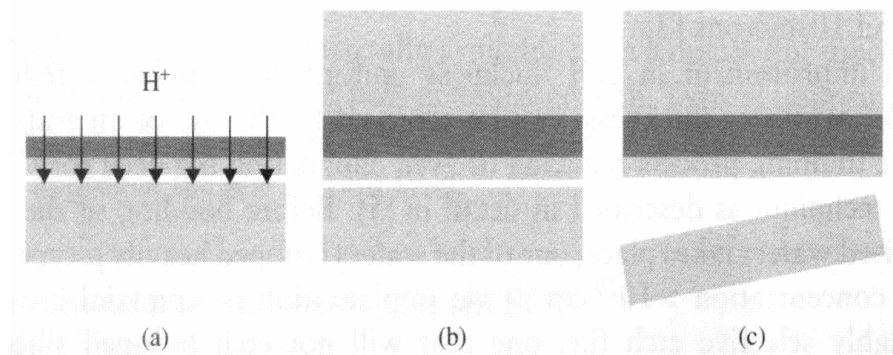


Figure 5.4 The SmartCut® process. (a) Thermally oxidized wafer is implanted with a high dose (approximately 10^{17} cm⁻²) of hydrogen. (b) A second wafer is bonded to the first as in the BESOI process. (c) Thermal processing splits the implanted wafer at a point consistent with the range of hydrogen ions

Wafer Splitting (SmartCut® Process to Produce Unibond® Wafers)

- Following implant, the wafer is brought into contact with a second, handling wafer (which may or may not have a thermal SiO₂-covered surface).
- Upon contact, room-temperature bonding occurs, such as that for the BESOI process.
- Subsequent thermal processing at 600°C and 1100°C first splits the implanted wafer along the peak of the hydrogen implantation profile, then strengthens the bond between the implanted and handling wafer.
- A fine CMP is employed to reduce roughness at the SOI surface.

Wafer Splitting (SmartCut® Process to Produce Unibond® Wafers)

- Subsequent epitaxial silicon growth can increase the thickness of the silicon overlayer if required.
- The nonuniformity of the position of the implanted hydrogen profile peak and hence the overlayer thickness are only a few percent. Importantly, although the overlayer receives a high dose implant, the small mass of the hydrogen ions ensures that negligible residual damage remains at the end of the thermal processing.
- A value for threading dislocations at a concentration $<10^2$ cm⁻² has been reported.

Wafer Splitting (SmartCut® Process to Produce Unibond® Wafers)

- The buried SiO₂ thickness is defined by the thermal oxidation process and hence may be varied from nanometers to several microns.
- The flexibility, high quality and efficient use of silicon offered by this process makes it an excellent platform for the development of low-cost silicon photonics.
- SOI wafers formed via the SmartCut® process are available commercially from SOITEC.

Silicon Epitaxial Growth

- “Epitaxial” means that the grown layer is an ordered mono-crystal, essential if efficient micro- or opto-electrical devices are to be fabricated.
- The use of epitaxial silicon as the waveguiding medium has the additional advantage of doping and defect levels below those found in wafers cut from an ingot following bulk growth using the Czochralski (Cz) or float zone (FZ) methods
- The most common epitaxial silicon growth technique is *chemical vapor deposition* (CVD).

Silicon Epitaxial Growth

- CVD is a process which deposits a solid film on the surface of a silicon wafer by the reaction of a gas mixture at that surface.
- For silicon deposition, dichlorosilane (SiH₂Cl₂) is often used as the source gas.
- It is a requirement that the wafer surface be raised in temperature (typically > 1000°C) to provide energy to drive the chemical reaction.
- Although either a vapor source or a solid source, as with molecular beam epitaxy (MBE), may be used, the desired thickness of the film required in silicon waveguide fabrication dictates that vapour phase epitaxy be dominant.
- The uniformity and repeatability of the commercially available machines and processes can result in thickness nonuniformities being less than 1 %

Deciding on the SOI

- SIMOX, BESOI and UniBond® have been used in the successful manufacture of silicon waveguides. However, there are differences in the SOI structures which should be considered at the commencement of a project.
- SIMOX-SOI
 - It has been commercially available for nearly two decades.
 - It is arguably the most researched structure of the three material types, and because it is based on an ion implantation process it is consistently reproducible in respect to quality and dimension.
 - Some concerns exist regarding the properties of the interface between the silicon overlayer and the buried oxide (i.e. micro-roughness) if SIMOX-SOI is to be used in the production of submicron waveguides, but this has yet to be quantified.
 - For the production of silicon overlayers greater than a few hundred nanometers, it is necessary to combine the SIMOX technique with silicon epitaxy

Deciding on the SOI

■ BESOI

- It has a silicon overlayer which has not been subjected to high-dose oxygen implantation, and the flexibility available in defining both the overlayer and the buried SiO₂ dimensions.
- Both BESOI and SIMOXSOI may be fabricated with thicknesses of several microns.
- Two start wafers are required to produce one SOI wafer using the BESOI process because of the inherent destructiveness of the thinning process.
⇒ In high-volume manufacture this can be a drawback.
- Without the use of an etch-stop, BESOI wafers have significantly greater nonuniformities than those produced via SIMOX and SmartCut®.

Deciding on the SOI

■ SmartCut® (Unibond® wafers)

- It combines the repeatability of an ion implantation process with the flexibility of BESOI in allowing the buried oxide thickness and silicon overlayer to be varied within wide dimensional limits (up to a few microns).
- This means that an epitaxial growth may not be necessary to form the waveguide structure if the desired maximum height of the silicon waveguide is less than approximately 2 μm.
- As with the SIMOX process, the silicon overlayer will have been subjected to a high-dose implantation, although the use of H⁺ as opposed to O⁺ ions reduces the risk of residual defects in the SOI structure.
- Unlike the BESOI process, the wafer from which the silicon overlayer is split can be recycled, so only one start wafer is required to produce one SOI wafer.

5.2 FABRICATION OF SURFACE ETCHED FEATURES

Photolithography

- The width of a rib waveguide is primarily determined by photolithographical definition, so control of the photo process is one of the most important challenges in silicon photonic fabrication.

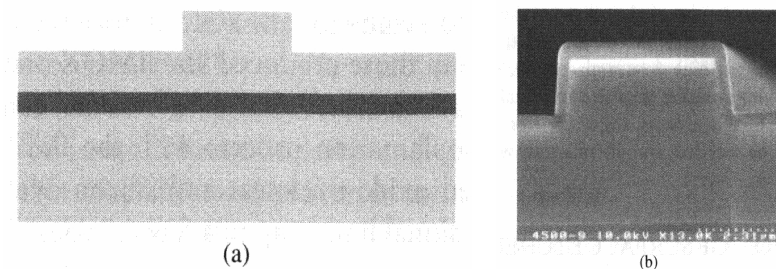


Figure 5.5 (a) Schematic of a silicon rib waveguide. (b) Electron micrograph of a silicon rib waveguide. Reproduced by permission of Intel Corporation

Photolithography

- Attainable minimum feature sizes are now well below 100 nm with **Critical Dimension (CD)** control at the 10 nm level.
- This kind of control is in excess of that required to form the most basic of silicon photonic structures such as the large-cross-section, single-mode silicon rib where minimum feature size is several microns and, by careful choice of the target dimensions, **CD** control can be relaxed to several hundred nanometers.

Photolithography

■ *Wafer Preparation*

- A necessary requirement before photolithography commences is that the wafer be free from particle contaminants and has been desorbed of any moisture.
- Ensuring the latter is especially important because wafer cleaning is via a wet process ending in a DI water rinse and dry.
- A dehydrated surface can be achieved by baking at a temperature above 150°C for several minutes prior to the application of photoresist.
- To complete the preparation, the wafer is coated with an adhesion promoter such as hexamethyldisilazane.

Photolithography

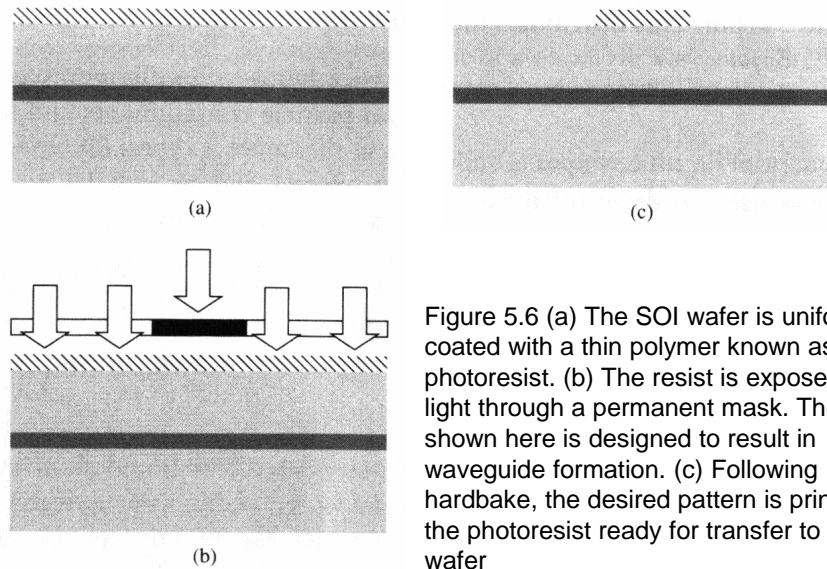
- However, the silicon photonics engineer may require the very best control available when fabricating more exotic devices or waveguides with dimensions which are submicron.
- Photolithography transfers a mask-defined pattern to the surface of a wafer.
- The pattern is printed on the wafer using a photosensitive polymer referred to as *photoresist*.
- Many recipes and process variations have been developed to ensure good, application-specific photolithography, but the underlying structure of all photo-processes is based on a number of common steps.

Photolithography

■ *Photoresist Application*

- The wafer is immediately coated with liquid photoresist following preparation.
- The resist is dispensed on the centre of the wafer which is held via a vacuum seal on a metal or polymer chuck.
- When approximately 1-10 ml of resist has been dispensed, the wafer is spun at a typical speed of between 1 and 5 krpm. This distributes the resist over the entire wafer surface (Figure 5.6a).

Photolithography



Photolithography

■ **Soft Bake**

- A post-spin soft bake is used to drive off most of the solvents in the resist while at the same time improving resist uniformity and adhesion. Typically, this is performed at 100°C for a few minutes.

■ **Exposure to Ultraviolet Light**

- The wafer is transferred to the mask-aligner where it is placed, with sub-micron precision, relative to the permanent pattern defined on the mask.

Photolithography

- Unless this is the first wafer layer, the pattern will be integrated with all previous layers. Once correctly aligned, the wafer is exposed to UV light (Figure 5.6b).
- In a **Positive Resist** process, the light passes through the transparent regions of the mask and activates the photosensitive components of the resist, such that these areas of resist are removed during the developing stage (see below).
- In a **Negative Resist** process the unexposed areas are removed.

Photolithography

■ **Photoresist Developing**

- The photoresist pattern is created at the developing stage during which the wafer is exposed to a developing solution.
- Whether the process is positive or negative, the solution dissolves the activated resist (or unactivated resist), leaving behind the resist pattern.

Photolithography

■ **Hardbake**

- The final hardbake drives off the remaining resist solvents and further strengthens the resist adhesion to the wafer surface. It is typically carried out at a temperature of 90-140 °C for up to several minutes.
- Although the bake temperature may vary significantly depending on the next process step to be undertaken, the upper limit must be such that the hardbake does not result in pattern deformation via resist flow.
- Following hardbake, the desired pattern is printed in the photoresist (Figure 5.6c).

Photolithography

- The photolithography process outlined in this section implies the use of the photoresist as the mask for the subsequent processing step.
- In some cases (for example silicon etching described below), it may be more appropriate to use a so-called “hard mask” such as silicon dioxide or silicon nitride.
- If this is the case, the photolithography process is used as a mask for etching of the thin dielectric layer, which is subsequently used as a hard mask.

Silicon Etching

- There are two general approaches:
 - ⇒ Wet etching and Dry etching.
- Each approach has advantages and disadvantages, but for reproducing features of submicron dimensions dry etching dominates.
- Low-loss silicon waveguides, having dimensions typically $> 1 \mu\text{m}$, have been produced by both wet and dry etching
- With the requirement for flexible process capability, tight tolerances and reproducible production,
 - ⇒ Dry etching is regarded as the most suitable solution.

Silicon Etching

- Dry etching proceeds through the formation of a low-pressure plasma (also used in deposition, photoresist removal, ion implantation, etc).
- A plasma is an ionized gas, virtually neutral overall, consisting of electrons, ions and mostly neutral particles.
- The formation of a localized plasma (such as that required for processing) can be achieved by the application of either DC or AC power to a process gas contained in an isolated chamber, although DC bias is rarely used in practice because it is incompatible with insulating electrodes causing surface charging and therefore an unstable plasma.
- AC bias circumvents this problem with charge build-up in one half-cycle, followed by charge neutralization in the next half.
- AC plasma generation therefore dominates in the design of semiconductor processing equipment, with the most common frequency being 13.56 MHz.

Silicon Etching

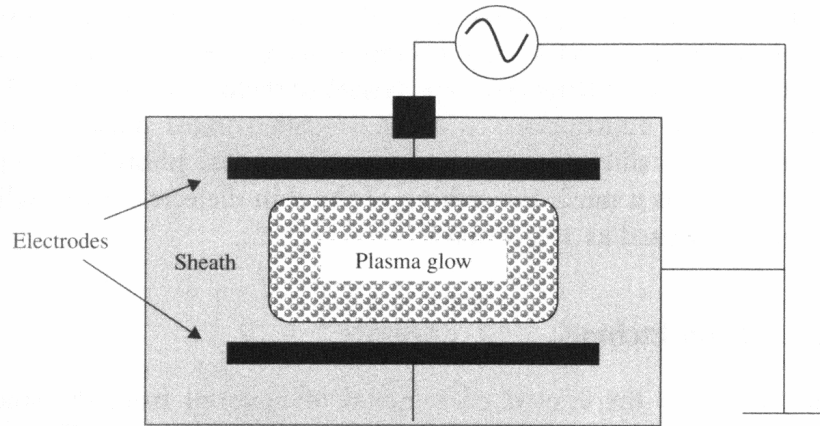


Figure 5.7 Schematic of a confined AC-generated plasma suitable for silicon processing. The processed wafer is placed on the lower, grounded electrode

Silicon Etching

- To begin the process, the plasma gas is introduced into the evacuated chamber and stabilized at a pressure between 10^{-3} and 10^{-2} Torr. Initial application of the AC signal causes free electrons in the gas to be accelerated greatly.
- These electrons lose energy through interaction with the gas atoms via processes such as molecular ionization and dissociation. The excited gas in turn gives rise to the emission of light and a distinctive glow is observed. The color of the glow is dependent on the elemental constituents of the gas.
- The vast disparity between the mass of the electrons and ions results in a time-averaged build-up of negative charge at the electrode surfaces, and a subsequent depletion of electrons in the gas volume close to the electrodes.

Silicon Etching

- Without electrons to drive the process, the excitation of the plasma gas in these volumes ceases and dark regions form (this is commonly referred to as a *sheath*).
- The average DC potential in the plasma chamber is determined by this distribution of charge.
- The result is an effective plasma potential (V_p), greater than the potential at either electrode, causing the acceleration of positively charged ions to the grounded electrode on which the process wafer is usually placed.
- The energy of ions is typically in the region of a few hundred electron-volts.

Silicon Etching

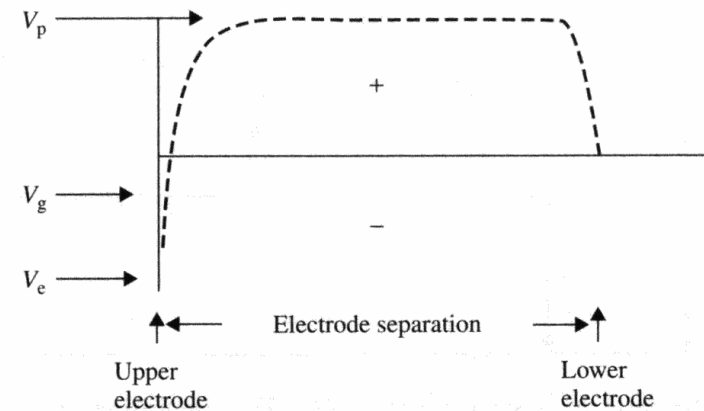


Figure 5.8 Representation of the time-averaged potential distribution in the plasma chamber. The labels "upper" and "lower" electrode refer to Figure 5.7. With the process wafer placed on the grounded (lower) electrode, singly charged ions arrive with an energy V_p

Silicon Etching

- A plasma used commonly in silicon processing is derived from CF_4 gas. CF_4 is normally stable, but dissociates (for example) into CF_3 , and F atoms in a plasma with the single fluorine atom being used as the active etch element for both Si and SiO_2 .
- A plasma based entirely on CF_4 would provide a slow etch rate owing to the swift recombination of CF_3 and F.
- By the addition of O_2 in the gas mix, the silicon etch rate can be dramatically increased owing to the reaction of oxygen with CF_3 inhibiting F recombination and hence increasing the free F concentration.
- Fluorine-based chemical reactions have formed the basis of many different silicon etching processes.
- This rather simplistic model of silicon dry-etching shields the reality of a set of complicated physical and chemical interactions.
- Plasma-based etchers are, however, ubiquitous in silicon processing and for a complete review of equipment and techniques the interested reader is referred to a more detailed text and references therein.

Silicon Etching

- *Reactive Ion Etch* (RIE).
- RIE is a technique that uses both chemical (reactive) and physical (sputtering) processes to remove material from the wafer surface.
- Unlike the generic etch chamber described above and shown in Figure 5.7, the wafer is positioned on the AC-driven electrode, which is significantly smaller than the grounded electrode. In this way, a large voltage develops between the plasma and the wafer, ensuring the plasma-generated reactive ions have a degree of directionality normal to the wafer surface.
- This in turn ensures preferential etching in the direction of acceleration. An important consideration in any silicon etching process (both wet and dry), but particularly for RIE, is the need for selectivity to the masking material.
- In general the greater the degree of physical etching used, the greater the erosion of the masking medium (usually photoresist).

Critical Dimension Control

- In fact, all of the steps in forming a silicon rib will effect a change in the dimensions of the rib, and each requires characterization and constant monitoring.
- In high-volume manufacture this will entail the use of *statistical process control* (SPC).
- The silicon overlayer thickness (h) is determined primarily by the process used to produce the SOI waveguiding layer.
- Silicon-on- SiO_2 lends itself particularly well to optical characterization, such as that performed with an infrared reflectometer or ellipsometer, and hence material may be screened easily prior to the fabrication of silicon photonic circuitry.

Critical Dimension Control

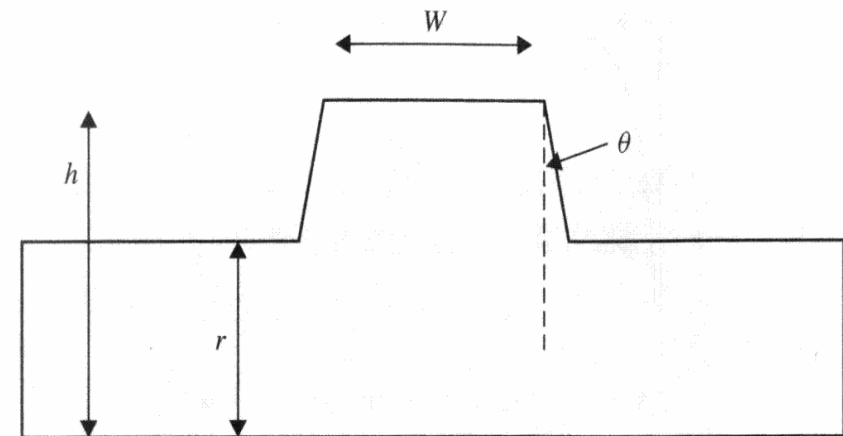


Figure 5.9 Schematic of a silicon waveguide. The dimensions critical to device performance are highlighted: rib width (W), silicon overlayer thickness (h), silicon thickness following rib etch (r) and rib wall angle (θ)

Critical Dimension Control

- The width of the rib (W) and the rib wall angle (θ) depend on both the photolithography and the silicon etch. In the case of W , a process bias will exist at each process step.
- For instance, the width of the rib image on the photo hard mask is generally different from that produced in the developed photoresist, and the ultimate width of the etched rib will be smaller than the photoresist image.
- The rib height ($h - r$) is determined by the dry silicon etch. Optical absorption and interferometric techniques exist allowing the in-situ determination of etch depth with a considerable degree of accuracy - so-called *end-point detection*.
- Subsequent to etch a useful method for measuring an etch depth of micron dimensions is via surface profilometry.

Critical Dimension Control

- Finally, an important consideration in calculating process bias for waveguides which have an upper oxide cladding is the reduction in h , r and W following thermal oxidation (see section 5.3).
- Because thermal oxidation proceeds via a reaction of oxygen and silicon atoms, the effect is a consumption of silicon and hence reduction of critical dimensions.
- A comparison of the atomic density of silicon ($5 \times 10^{22} \text{ cm}^{-3}$) and the molecular density of SiO_2 ($2.2 \times 10^{22} \text{ cm}^{-3}$) leads immediately to the fact that, for the growth of a given thickness t of SiO_2 , a thickness of silicon equal to $(0.44 t)$ is consumed.