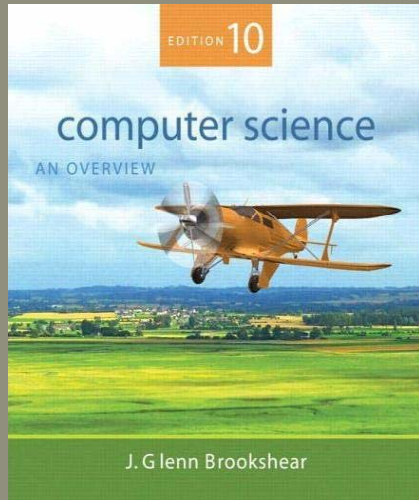
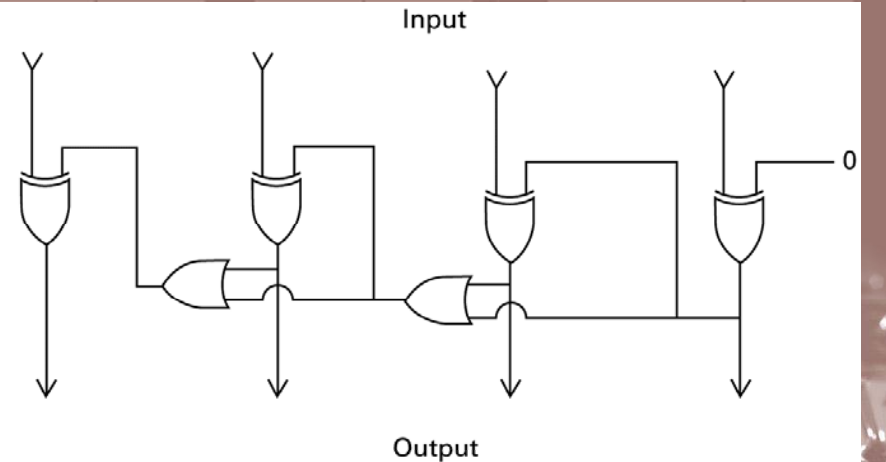


# Appendices



**Figure B.1** A circuit that negates a two's complement pattern



Bqq.4



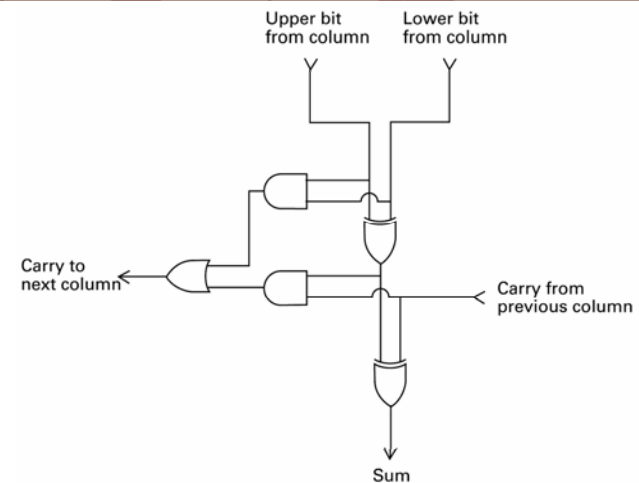
**Appendix A: Samples from ASCII**

| Symbol | ASCII    | Symbol    | ASCII    |
|--------|----------|-----------|----------|
| A      | 01000001 | 0         | 00110000 |
| B      | 01000010 | 1         | 00110001 |
| C      | 01000011 | 2         | 00110010 |
| a      | 01100001 | #         | 00100011 |
| b      | 01100010 | .         | 00101110 |
| c      | 01100011 | line feed | 00001010 |

Bqq.3



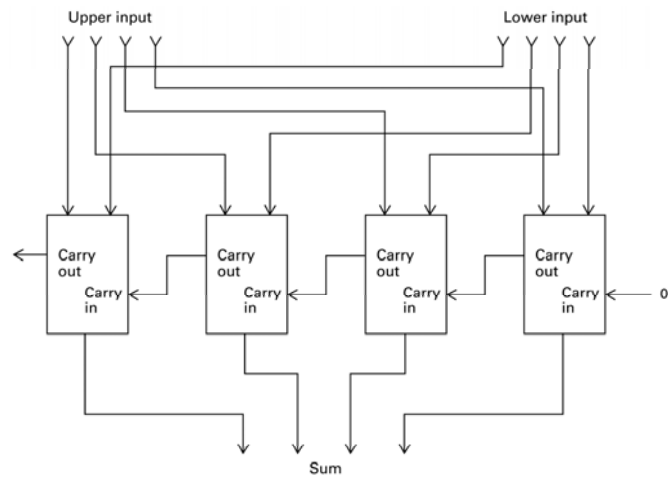
**Figure B.2** A circuit to add a single column



Bqq.5



Figure B.3 A circuit for adding two's complement values



Bqq.6



Appendix C: A Simple Machine Language (continued)

| Op-code | Operand | Description               |
|---------|---------|---------------------------|
| 7       | RST     | OR S and T into R.        |
| 8       | RST     | AND S and T into R.       |
| 9       | RST     | XOR S and T into R.       |
| A       | ROX     | ROTATE reg. R X times.    |
| B       | RXY     | JUMP to XY if R = reg. 0. |
| C       | 000     | HALT.                     |

Bqq.8



Appendix C: A Simple Machine Language

| Op-code | Operand | Description                        |
|---------|---------|------------------------------------|
| 1       | RXY     | LOAD reg. R from cell XY.          |
| 2       | RXY     | LOAD reg. R with XY.               |
| 3       | RXY     | STORE reg. R at XY.                |
| 4       | ORS     | MOVE R to S.                       |
| 5       | RST     | ADD S and T into R. (2's comp.)    |
| 6       | RST     | ADD S and T into R. (floating pt.) |

Bqq.7